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DOCKET NO. 6926-007-20 CONT

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

TRANSMITTED HEREWITH FOR FILING IS THE PATENT APPLICATION OF:

INVENTOR(S): H. BRITTON SANDERFORD AND ROBERT E. ROUQUETTE

FOR: WIRELESS ALARM SYSTEM

ENCLOSED ARE:

■ EIGHT SHEETS OF DRAWINGS.

☐ A CERTIFIED COPY OF A _____ APPLICATION.

☐ AN ASSIGNMENT OF THE INVENTION TO _____.

☐ A VERIFIED STATEMENT TO ESTABLISH SMALL ENTITY STATUS UNDER 37 CFR 1.27.

■ ALSO ENCLOSED: PRELIMINARY AMENDMENT
LIST OF INVENTORS' NAMES AND ADDRESSES

THE FILING FEE IS CALCULATED BELOW:

CLAIMS	(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) CALCULATIONS
	TOTAL CLAIMS	120 -20 =	100	X $ 22 =	$2,200.00
	INDEPENDENT	17 - 3 =	14	X $ 80 =	$1,120.00
	MULTIPLE DEPENDENT CLAIMS (if applicable)			+ $260 =	$ 260.00
	LATE FILING OF DECLARATION			+ $130 =	$ 130.00
			BASIC FEE		$ 770.00
			TOTAL OF ABOVE CALCULATIONS =		$4,480.00
	Reduction by 50% for filing by Small Entity				
	☐ FILING IN NON-ENGLISH LANGUAGE			+ $130 =	$
	☐ RECORDATION OF ASSIGNMENT			+ $ 40 =	$
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6926-007-20 CONT

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE:

H. Britton SANDERFORD, et al. : GROUP: UNASSIGNED

SERIAL NO. NEW APPLICATION :

FILED: HEREWITH : EXAMINER: UNASSIGNED

FOR: WIRELESS ALARM SYSTEM :

LETTER

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

Listed below are the names and addresses of the inventors for the above-identified patent application.

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New Orleans, Louisiana 70124

Robert E. ROUQUETTE
633 Meursault Drive
Kenner, Louisiana 70065

A Declaration containing all the necessary information will be submitted at a later date.

Respectfully submitted,

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(OSMMN 4/95)

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IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE:

H. Britton SANDERFORD, et al. : GROUP: UNASSIGNED

SERIAL NO. NEW APPLICATION :

FILED: HEREWITH : EXAMINER: UNASSIGNED

FOR: WIRELESS ALARM SYSTEM :

PRELIMINARY AMENDMENT

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

Prior to examination, please amend the above-identified application as follows:

IN THE SPECIFICATION

Title page, line 5, delete "and"; and

line 6, delete "JAMES D. ARTHUR".

Page 1, after line 4, insert

--CROSS REFERENCE TO RELATED APPLICATION

This application is a continuation of U.S. patent application Serial No. 08/08/487,523 filed June 7, 1995 entitled Wireless Alarm System which is a continuation of application 07/782,345 (filed 10/24/91) revived, which is a divisional of 07/569,682 (filed 08/20/90), now U.S. Patent 5,095,493, which is a divisional of 07/266,461 (filed 11/02/88), now U.S. Patent 4,977,577.--

IN THE CLAIMS

Please cancel without prejudice Claims 1-64.

Please add new Claims 65-101 as follows:

--65. A remote power meter monitoring system, comprising:

a multiplicity of radio frequency transmit-only devices configured to transmit information, each radio frequency transmit-only device comprising,

a timer comprising a memory that holds a pseudo random time interval value, said timer configured to autonomously initiate transmission of said information after expiration of a time duration corresponding to said pseudo random time interval value held in said memory,

a pseudo-randomization means for generating and loading said pseudo random time interval value into said timer, and

a retransmission means for redundantly transmitting said information a predetermined number of times;

at least one sensing element configured to provide sensor data to said radio frequency transmit-only device, said transmitted information comprising said sensor data, an identification address being assigned to said radio frequency transmit-only device to which the sensor data is provided, and error detection code bits;

at least two receivers each configured to receive said transmitted information, and configured to validate said information based on said identification address and said error detection code bits contained in said transmitted information, said receivers providing redundant reception of said transmitted

information; and

a monitoring means for monitoring said information as received and validated by at least one of said receivers.

66. A remote power meter monitoring system, comprising:

a multiplicity of radio frequency transmit-only devices configured to transmit information in a direct sequence spread spectrum signal at plural frequencies, each radio frequency transmit-only device comprising,

a processor configured to generate said information to be transmitted,

a crystal oscillator configured to generate spread spectrum timing for said information generated by said processor,

a timer configured to hold a pseudo random time interval value, said timer configured to initiate transmission of said information after expiration of a time duration corresponding to said pseudo random time interval value,

a pseudo-randomization means for generating and loading said pseudo random time interval value into said timer,

a retransmission means for redundantly transmitting said information a predetermined number of times, and

a wake-up circuit configured to initiate said crystal oscillator and said processor in respective active states upon expiration of said time duration so as to transmit said information, and configured to place said crystal oscillator and said processor in a reduced current state between transmissions;

at least one sensing element configured to provide sensor

data to said radio frequency transmit-only device, said transmitted information comprising said sensor data, an identification address being assigned to said radio frequency transmit-only device to which the sensor data is provided, and error detection code bits;

at least two receivers each configured to receive said transmitted information, and configured to validate said information based on said identification address and said error detection code bits contained in said transmitted information, said receivers providing redundant reception of said transmitted information; and

a monitoring means for monitoring said information as received and validated by at least one of said receivers.

67. A remote power meter monitoring system, comprising:

a multiplicity of radio frequency transmit-only devices configured to transmit information in a direct sequence spread spectrum signal at plural frequencies, said information comprising a first field comprising a preamble configured to establish chip code timing synchronization and a second field comprising data, said first field being transmitted prior to said second field, said preamble having a length measured in bit times that is at least equal in length to a number of chips in a chip code sequence used to produce said spread spectrum signal, each radio frequency transmit-only device comprising,

a timer comprising a memory for holding a pseudo random time interval value, said timer configured to autonomously

initiate transmission of said information after expiration of a time duration corresponding to said pseudo random time interval value held in said memory,

a pseudo-randomization means for generating and loading said pseudo random time interval value into said timer, and

a retransmission means for redundantly transmitting said information a predetermined number of times;

at least one sensing element configured to provide sensor data to said radio frequency transmit-only device, said transmitted information comprising said sensor data, an identification address being assigned to said radio frequency transmit-only device to which the sensor data is provided, and error detection code bits;

at least two receivers each configured to receive said transmitted information, and configured to validate said information based on said identification address and said error detection code bits contained in said transmitted information, said at least two receivers providing redundant reception of said transmitted information, said at least two receivers configured to establish chip code synchronization to said direct sequence spread spectrum signal using said preamble; and

a monitoring means for monitoring said information as received and validated by at least one of said receivers.

68. A remote power meter monitoring system, comprising:

a multiplicity of radio frequency transmit-only devices

configured to transmit information in a direct sequence spread spectrum signal at plural frequencies, said information comprising a first field comprising a preamble configured to establish chip code timing synchronization and a second field comprising data, said first field being transmitted prior to said second field, said preamble having a length measured in bit times that is at least equal in length to a number of chips in a chip code sequence plus approximately five bit times, each radio frequency transmit-only device comprising,

a timer comprising a memory for holding a pseudo random time interval value, said timer configured to autonomously initiate transmission of said information after expiration of a time duration corresponding to said pseudo random time interval value held in said memory,

a pseudo-randomization means for generating and loading said pseudo random time interval value into said timer, and

a retransmission means for redundantly transmitting said information a predetermined number of times;

at least one sensing element configured to provide sensor data to said radio frequency transmit-only device, said transmitted information comprising said sensor data, an identification address being assigned to said radio frequency transmit-only device to which the sensor data is provided, and error detection code bits;

at least two receivers each configured to receive said transmitted information, and configured to validate said

information based on said identification address and said error detection code bits contained in said transmitted information, said receivers providing redundant reception of said transmitted information, said receivers configured to establish chip code lock and fine chip code synchronization using said preamble; and

a monitoring means for monitoring said information as received and validated by at least one of said receivers.

69. A remote power meter monitoring system, comprising:

a multiplicity of radio frequency transmit-only devices configured to transmit information in a direct sequence spread spectrum signal at plural frequencies, said information comprising a first field comprising a preamble configured to establish chip code timing synchronization and a second field comprising data, said first field being transmitted prior to said second field, said preamble having a length measured in bit times that is less than n bit times, where n equals a number of chips in a chip code sequence, each radio frequency transmit-only device comprising,

a timer comprising a memory for holding a pseudo random time interval value, said timer configured to autonomously initiate transmission of said information after expiration of a time duration corresponding to said pseudo random time interval value held in said memory,

a pseudo-randomization means for generating and loading said pseudo random time interval value into said timer, and

a retransmission means for redundantly transmitting

said information a predetermined number of times;

at least one sensing element configured to provide sensor data to said radio frequency transmit-only device, said transmitted information comprising said sensor data, an identification address being assigned to said radio frequency transmit-only device to which the sensor data is provided, and error detection code bits;

at least two receivers each configured to receive said transmitted information, and configured to validate said information based on said identification address and said error detection code bits contained in said transmitted information, said receivers providing redundant reception of said transmitted information, said receivers comprising respective parallel correlation means for establishing chip code synchronization using said preamble; and

a monitoring means for monitoring said information as received and validated by at least one of said receivers.

70. A remote power meter monitoring system, comprising:

a multiplicity of radio frequency transmit-only devices configured to transmit information in a direct sequence spread spectrum signal at plural frequencies, each radio frequency transmit-only device comprising,

a processor configured to generate said information to be transmitted,

a crystal oscillator configured to generate spread spectrum timing for said information generated by said processor,

a timer configured to delay transmission of said information by a predetermined delay after said expiration of said time duration so as to allow for crystal stabilization, transmit carrier frequency stabilization and chip code timing generation stabilization,

a retransmission means for redundantly transmitting said information a predetermined number of times, and

a wake-up circuit configured to initiate said crystal oscillator and said processor in respective active states upon expiration of said time duration so as to transmit said information, and configured to place said crystal oscillator and said processor in a reduced current state between transmissions;

at least one sensing element configured to provide sensor data to said radio frequency transmit-only device, said transmitted information comprising said sensor data, an identification address being assigned to said radio frequency transmit-only device to which the sensor data is provided, and error detection code bits;

at least two receivers each of which being configured to receive said transmitted information, and configured to validate said information based on said identification address and said error detection code bits contained in said transmitted information, said receivers providing redundant reception of said transmitted information; and

a monitoring means for monitoring said information as received and validated by at least one of said receivers.

71. The system according to Claims 66, 67, 68, or 69, wherein respective of said radio frequency transmit-only devices, further comprises:

a processor configured to generate said information to be transmitted,

a crystal oscillator configured to generate spread spectrum timing for said information generated by said processor,

an oscillator configured to generate a carrier on which said information to be transmitted is modulated;

a wake-up circuit configured to initiate said crystal oscillator and said oscillator in respective active states upon expiration of said time duration so as to transmit said information, and configured to place said crystal oscillator and said oscillator in a reduced current state between transmissions, said information being transmitted after a predetermined delay with respect to when said crystal oscillator and said oscillator are placed in said respective active states so as to allow for stabilization in said oscillator and said crystal oscillator prior to information transmission.

72. The system according to Claims 67, 68, 69, or 70, wherein a chip code sequence used to produce said preamble is a same sequence as a data bearing chip code sequence.

73. A remote power meter monitoring system, comprising:

a multiplicity of radio frequency transmit-only devices configured to transmit information, each radio frequency transmit-

only device comprising,

a timer configured to autonomously initiate transmission of said information after expiration of a time duration, and

a pseudo-randomization means for randomizing the time interval between transmissions of said message,

a retransmission means for redundantly transmitting said message a predetermined number of times,

a processor configured to generate said information to be transmitted,

a crystal oscillator configured to generate spread spectrum timing for said information generated by said processor,

a carrier generator mechanism configured to generate a carrier on which said information to be transmitted is modulated, and

a wake-up circuit configured to initiate said crystal oscillator and said carrier generator mechanism in respective active states upon expiration of said time duration so as to transmit said information, and configured to place said crystal oscillator and said carrier generator mechanism in a reduced current state between transmissions, said information being transmitted after a predetermined delay with respect to when said crystal oscillator and said carrier generator mechanism are placed in said respective active states so as to allow for stabilization in said carrier generator mechanism and said crystal oscillator prior to information transmission;

at least one sensing element configured to provide sensor

data to said radio frequency transmit-only device, said transmitted information comprising said sensor data, an identification address being assigned to said radio frequency transmit-only device to which the sensor data is provided, and error detection code bits;

a receiver configured to receive said transmitted information, and configured to validate said information based on said identification address and said error detection code bits contained in said transmitted information; and

a monitoring means for monitoring said information as received and validated by said receiver.

74. A remote power meter monitoring system, comprising:

a multiplicity of radio frequency transmit-only devices configured to transmit information in a direct sequence spread spectrum signal at plural frequencies, each radio frequency transmit-only device comprising,

a processor configured to generate said information to be transmitted,

a crystal oscillator configured to generate spread spectrum timing for said information generated by said processor,

a timer configured to initiate transmission of said information after expiration of a time duration,

a retransmission means for redundantly transmitting said information a predetermined number of times,

a pseudo-randomization means for randomizing the time interval between redundant transmissions,

a processor configured to generate said information to be transmitted,

a crystal oscillator configured to generate spread spectrum timing for said information generated by said processor,

a carrier generator mechanism configured to generate a carrier on which said information to be transmitted is modulated, and

a wake-up circuit configured to initiate said crystal oscillator and said carrier generator mechanism in respective active states upon expiration of said time duration so as to transmit said information, and configured to place said crystal oscillator and said carrier generator mechanism in a reduced current state between transmissions, said information being transmitted after a predetermined delay with respect to when said crystal oscillator and said carrier generator mechanism are placed in said respective active states so as to allow for stabilization in said carrier generator mechanism and said crystal oscillator prior to information transmission;

at least one sensing element configured to provide sensor data to said radio frequency transmit-only device, said transmitted information comprising said sensor data, an identification address being assigned to said radio frequency transmit-only device to which the sensor data is provided, and error detection code bits;

a receiver configured to receive said transmitted information, and configured to validate said information based on said identification address and said error detection code bits

contained in said transmitted information; and

a monitoring means for monitoring said information as received and validated by said receiver.

75. A remote power meter monitoring system, comprising:

a multiplicity of radio frequency transmit-only devices configured to transmit information in a direct sequence spread spectrum signal at plural frequencies, said information comprising a first field comprising a preamble configured to establish chip code timing synchronization and a second field comprising data, said first field being transmitted prior to said second field, said preamble having a length measured in bit times that is at least equal in length to a number of chips in a chip code sequence used to produce said spread spectrum signal, each radio frequency transmit-only device comprising,

a timer configured to autonomously initiate transmission of said information after expiration of a time duration,

a retransmission means for redundantly transmitting said information a predetermined number of times,

a pseudo-randomization means for randomizing the time interval between redundant transmissions,

a processor configured to generate said information to be transmitted,

a crystal oscillator configured to generate spread spectrum timing for said information generated by said processor,

a carrier generator mechanism configured to generate

a carrier on which said information to be transmitted is modulated, and

a wake-up circuit configured to initiate said crystal oscillator and said carrier generator mechanism in respective active states upon expiration of said time duration so as to transmit said information, and configured to place said crystal oscillator and said carrier generator mechanism in a reduced current state between transmissions, said information being transmitted after a predetermined delay with respect to when said crystal oscillator and said carrier generator mechanism are placed in said respective active states so as to allow for stabilization in said carrier generator mechanism and said crystal oscillator prior to information transmission;

at least one sensing element configured to provide sensor data to said radio frequency transmit-only device, said transmitted information comprising said sensor data, an identification address being assigned to said radio frequency transmit-only device to which the sensor data is provided, and error detection code bits;

a receiver configured to receive said transmitted information, and configured to validate said information based on said identification address and said error detection code bits contained in said transmitted information, said receiver configured to establish chip code synchronization to said direct sequence spread spectrum signal using said preamble; and

a monitoring means for monitoring said information as received and validated by said receiver.

76. A remote power meter monitoring system, comprising:

a multiplicity of radio frequency transmit-only devices configured to transmit information in a direct sequence spread spectrum signal at plural frequencies, said information comprising a first field comprising a preamble configured to establish chip code timing synchronization and a second field comprising data, said first field being transmitted prior to said second field, said preamble having a length measured in bit times that is at least equal in length to a number of chips in a chip code sequence plus approximately five bit times, each radio frequency transmit-only device comprising,

a timer configured to autonomously initiate transmission of said information after expiration of a time duration,

a retransmission means for redundantly transmitting said information a predetermined number of times,

a pseudo-randomization means for randomizing the time interval between redundant transmissions,

a processor configured to generate said information to be transmitted,

a crystal oscillator configured to generate spread spectrum timing for said information generated by said processor,

a carrier generator mechanism configured to generate a carrier on which said information to be transmitted is modulated, and

a wake-up circuit configured to initiate said crystal oscillator and said carrier generator mechanism in

respective active states upon expiration of said time duration so as to transmit said information, and configured to place said crystal oscillator and said carrier generator mechanism in a reduced current state between transmissions, said information being transmitted after a predetermined delay with respect to when said crystal oscillator and said carrier generator mechanism are placed in said respective active states so as to allow for stabilization in said carrier generator mechanism and said crystal oscillator prior to information transmission;

at least one sensing element configured to provide sensor data to said radio frequency transmit-only device, said transmitted information comprising said sensor data, an identification address being assigned to said radio frequency transmit-only device to which the sensor data is provided, and error detection code bits;

a receiver configured to receive said transmitted information, and configured to validate said information based on said identification address and said error detection code bits contained in said transmitted information, said receiver configured to establish chip code lock and fine chip code synchronization using said preamble; and

a monitoring means for monitoring said information as received and validated by said receiver.

77. A remote power meter monitoring system, comprising:

a multiplicity of radio frequency transmit-only devices configured to transmit information in a direct sequence spread

spectrum signal at plural frequencies, said information comprising a first field comprising a preamble configured to establish chip code timing synchronization and a second field comprising data, said first field being transmitted prior to said second field, said preamble having a length measured in bit times that is less than n bit times, where n equals a number of chips in a chip code sequence, each radio frequency transmit-only device comprising,

a timer configured to autonomously initiate transmission of said information after expiration of a time duration,

a retransmission means for redundantly transmitting said information a predetermined number of times,

a pseudo-randomization means for randomizing the time interval between redundant transmissions,

a processor configured to generate said information to be transmitted,

a crystal oscillator configured to generate spread spectrum timing for said information generated by said processor,

a carrier generator mechanism configured to generate a carrier on which said information to be transmitted is modulated, and

a wake-up circuit configured to initiate said crystal oscillator and said carrier generator mechanism in respective active states upon expiration of said time duration so as to transmit said information, and configured to place said crystal oscillator and said carrier generator mechanism in a reduced current state between transmissions, said information

being transmitted after a predetermined delay with respect to when said crystal oscillator and said carrier generator mechanism are placed in said respective active states so as to allow for stabilization in said carrier generator mechanism and said crystal oscillator prior to information transmission;

at least one sensing element configured to provide sensor data to said radio frequency transmit-only device, said transmitted information comprising said sensor data, an identification address being assigned to said radio frequency transmit-only device to which the sensor data is provided, and error detection code bits;

a receiver configured to receive said transmitted information, and configured to validate said information based on said identification address and said error detection code bits contained in said transmitted information, said receiver comprising respective parallel correlation means for establishing chip code synchronization using said preamble; and

a monitoring means for monitoring said information as received and validated by said receiver.

78. The system according to Claims 65, 66, 67, 68, 69, 70, 73, 74, 75, 76, or 77, wherein said radio frequency transmit-only device comprises an information priority mechanism that is configured to increase a rate of information transmission when said sensor data input to said radio frequency transmit-only device changes.

79. The system according to Claims 65, 66, 67, 68, 69, 70, 73, 74, 75, 76, or 77, wherein said radio frequency transmit-only device further comprises:

a transmitter oscillator having an enable input being configured to generate a carrier on which said information is carried;

a power amplifier having an enable input and being configured to amplify said carrier prior to transmission of said information which modulates said carrier; and

an enabling device connected to said enable input of said transmitter oscillator and said enable input of said power amplifier configured to enable an active state of said transmitter oscillator and said power amplifier during periods of information transmission and configured to place said transmitter oscillator and said power amplifier in a low current state during periods of non-transmission, thereby reducing current drain.

80. The system according to Claims 65, 66, 67, 68, 69, 70, 73, 74, 75, 76, or 77, wherein said radio frequency transmit-only device further comprises:

a processor configured to generate said information to be transmitted; and

a wake-up circuit that maintains said processor in a reduced current state between transmissions, and upon expiration of said time duration, as determined by said timer, places said processor in a normal operational state.

81. The system according to Claims 65, 66, 70, 73, or 74, wherein said radio frequency transmit-only device comprises a programming connector means for assigning said identification address to said radio frequency transmit-only device using a serial data stream.

82. The system according to Claim 81, further comprising a hand held terminal configured to load said identification address in the serial data stream to said programming connector.

83. The system according to Claims 65, 66, 70, 73, or 74, wherein said timer is configured to divide said time duration into a very fine number of temporal time slots.

84. The system according to Claims 65, 70, 73, or 74, wherein said radio frequency transmit-only device includes a programming connector means for assigning through a serial data stream said identification address, a type code, and a code division multiple access channel on which said radio frequency transmit-only device is to operate.

85. The system according to Claims 66, 67, 70, 74, or 75, wherein said radio frequency transmit-only device comprises a data rate between 14 Kb/s and 21 Kb/s and a chip rate between 1.0 Mc/s and 1.3 Mc/s.

86. The system according to Claims 65, 66, 67, 68, 69, 70,

73, 74, 75, 76, or 77 wherein said pseudo-randomization means is configured to be seeded with said identification address so as to prevent repeat collisions.

87. A remote power meter monitoring method, comprising the steps of:

retrieving data from a sensing element;

generating information containing the retrieved data, comprising,

generating an identification address field for holding an identification address corresponding to a transmit-only device, and

generating an error correction code;

transmitting the generated information, redundantly at pseudo random intervals from said transmit-only device, comprising,

loading a timer with a pseudo random time interval value,

enabling, upon expiration of said timer, a crystal oscillator used to generate spread spectrum timing signals, a transmitter oscillator used to generate transmission signals,

delaying information transmission for a predetermined time period, relative to said expiration of said time interval, to allow for stabilization of said crystal oscillator and said transmitter oscillator,

transmitting a preamble portion of said information used for spread spectrum timing synchronization, said preamble having a length in bit times at least equal to a number of chips

in a chip code sequence used in direct sequence spread spectrum format by said transmit-only device,

transmitting the generated information in said direct sequence spread spectrum format based upon said chip code sequence and said spread spectrum timing signals at a predetermined frequency by said transmit-only device,

disabling said crystal oscillator and said transmitter oscillator, so as to conserve power;

repeating said step of transmitting said generated information redundantly after a pseudorandom interval of time so as to provide information transmission redundancy;

receiving the generated information by at least one receiver;

validating the received information based on said identification address and said error correction code;

transferring the validated information to a monitoring mechanism; and

monitoring the received data in the validated information with the monitoring mechanism.

88. The method of Claim 87, wherein said step of generating information, comprises generating said information to have a data rate of approximately 14 Kb/s to 21 Kb/s and a chip rate of approximately 1 Mc/s to 1.3 Mc/s.

89. The method according to Claim 87, further comprising the step of programming said identification address into said transmit-only device via a programming connector prior to

installing said transmit-only device.

90. The method according to Claims 87 or 88, wherein said step of transmitting said generated information, redundantly comprises the substep of generating said preamble using a preamble chip code that is a same chip code sequence as that used with said received data.

91. A remote power meter monitoring system, comprising:

a multiplicity of radio frequency transmit-only devices configured to transmit information, each radio frequency transmit-only device comprising,

a timer configured to autonomously initiate transmission of said information after expiration of a time duration,

a random number generator configured to generate said pseudo random time interval value and to cause the time interval between transmissions to be pseudorandom, and

a retransmission mechanism configured to retransmit said information a predetermined number of times;

at least one sensing element configured to provide sensor data gathered therein to said radio frequency transmit-only device, said transmitted information comprising said sensor data, an identification address being assigned to said radio frequency transmit-only device to which the sensor data is provided, and error detection code bits;

at least two receivers configured to receive said transmitted

information, and configured to validate said information based on said identification address and said error detection code bits contained in said transmitted information, said receivers providing redundant reception of said transmitted information; and

a monitoring apparatus that is configured to monitor said information as received and validated by at least one of said receivers.

92. A remote power meter monitoring system, comprising:

a multiplicity radio frequency transmit-only devices configured to transmit information in a direct sequence spread spectrum signal at plural frequencies, each radio frequency transmit-only device comprising,

a processor configured to generate said information to be transmitted,

a crystal oscillator configured to generate spread spectrum timing information for said information generated by said processor,

a timer configured to hold a pseudo random time interval value and initiate transmission of said information after expiration of a time duration corresponding to said pseudo random time interval value,

a random number generator mechanism that generates said pseudo random time interval value and loads said pseudo random time interval value into said timer, and

a retransmission mechanism configured to cause said information to be retransmitted a predetermined number of times,

and

a wake-up circuit configured to initiate said crystal oscillator and said processor in respective active states upon expiration of said time duration so as to transmit said information when in said respective active states, and configured to place said crystal oscillator and said processor in a reduced current state between transmission times;

at least one sensing element configured to provide sensor data to said radio frequency transmit-only device, said transmitted information comprising,

a data field that holds said sensor data,

an address field that holds an identification address being assigned to said radio frequency transmit-only device to which the sensor data is provided, and

an error field that holds error detection code bits;

at least two receivers each configured to receive said transmitted information, and configured to validate said information based on said identification address and said error detection code bits contained in said transmitted information, said receivers providing redundant reception of said transmitted information; and

a monitoring apparatus that is configured to monitor said information as received and validated by at least one of said receivers.

93. A remote power meter monitoring system, comprising:

a multiplicity of radio frequency transmit-only devices

configured to transmit information in a direct sequence spread spectrum signal at plural frequencies, said information comprising a first field comprising a preamble configured to establish chip code timing synchronization and a second field comprising data, said first field being transmitted prior to said second field, said preamble having a length measured in bit times that is at least equal in length to a number of chips in a chip code sequence used to produce said spread spectrum signal, each radio frequency transmit-only device comprising,

a timer configured to autonomously initiate transmission of said information after expiration of a time duration,

a random number generator that generates said pseudo random time interval value and causes the time interval between transmissions to be psudeorandom, and

a retransmission mechanism configured to cause said information to be retransmitted a predetermined number of times;

at least one sensing element configured to provide sensor data to said radio frequency transmit-only device, said transmitted information comprising,

a data field that holds said sensor data,

an address field that holds an identification address being assigned to said radio frequency transmit-only device to which the sensor data is provided, and

an error field that holds error detection code bits;

at least two receivers each configured to receive said transmitted information, and configured to validate said

information based on said identification address and said error detection code bits contained in said transmitted information, said receivers providing redundant reception of said transmitted information, said receivers configured to establish chip code synchronization to said direct sequence spread spectrum signal using said preamble; and

a monitoring apparatus that is configured to monitor said information as received and validated by at least one of said receivers.

94. A remote power meter monitoring system, comprising:

a multiplicity of radio frequency transmit-only devices configured to transmit information in a direct sequence spread spectrum signal at plural frequencies, said information comprising a first field comprising a preamble configured to establish chip code timing synchronization and a second field comprising data, said first field being transmitted prior to said second field, said preamble having a length measured in bit times that is at least equal in length to a number of chips in a chip code sequence plus approximately five bit times, each radio frequency transmit-only device comprising,

a timer comprising a memory that holds a pseudo random time interval value, and configured to autonomously initiate transmission of said information after expiration of a time duration corresponding to said pseudo random time interval value held in said memory,

a random number generator configured to generate

said pseudo random time interval value and load said pseudo random time interval value into said timer, and

a retransmission device for redundantly transmitting said information a predetermined number of times;

at least one sensing element configured to provide sensor data to said radio frequency transmit-only device, said transmitted information comprising said sensor data, an identification address being assigned to said radio frequency transmit-only device to which the sensor data is provided, and error detection code bits;

at least two receivers each configured to receive said transmitted information, and configured to validate said information based on said identification address and said error detection code bits contained in said transmitted information, said receivers providing redundant reception of said transmitted information, said receivers configured to establish chip code lock and fine chip code synchronization using said preamble; and

a monitoring device for monitoring said information as received and validated by at least one of said receivers.

95. A remote power meter monitoring system, comprising:

a multiplicity of radio frequency transmit-only devices configured to transmit information in a direct sequence spread spectrum signal at plural frequencies, said information comprising a first field comprising a preamble configured to establish chip code timing synchronization and a second field comprising data, said first field being transmitted prior to said second field,

said preamble having a length measured in bit times that is less than n bit times, where n equals a number of chips in a chip code sequence, each radio frequency transmit-only device comprising,

a timer comprising a memory that holds a pseudo random time interval value, said timer configured to autonomously initiate transmission of said information after expiration of a time duration corresponding to said pseudo random time interval value held in said memory,

a random number generator configured to generate said pseudo random time interval value and for loading said pseudo random time interval value into said timer, and

a retransmission device for redundantly transmitting said information a predetermined number of times;

at least one sensing element configured to provide sensor data to said radio frequency transmit-only device, said transmitted information comprising,

a data field that holds said sensor data,

an address field that holds an identification address being assigned to said radio frequency transmit-only device to which the sensor data is provided, and

an error field that holds error detection code bits;

at least two receivers each configured to receive said transmitted information, and configured to validate said information based on said identification address and said error detection code bits contained in said transmitted information, said receivers providing redundant reception of said transmitted information, said receivers comprising respective parallel

correlation mechanisms that establish chip code synchronization using said preamble; and

a monitoring device for monitoring said information as received and validated by at least one of said receivers.

96. The system according to Claims 91, 92, 93, 94 or 95, wherein said radio frequency transmit-only device comprises a program connector through which said identification address is input in a serial data stream format.

97. The system according to Claims 91, 92, 93, 94, or 95, wherein said radio frequency transmit-only device includes a program connector through which said identification address, a type code, and a code division multiple access channel on which said radio frequency transmit-only device is to operate are input in a serial data stream.

98. The system according to Claims 91, 92, 93, or 95, wherein said random number generator is configured to be seeded with said identification address so as to prevent repeat collisions.

99. The system according to Claims 93, 94, or 95, wherein said timer is configured to delay transmission of said information to be transmitted by a predetermined delay after said expiration of said time duration so as to allow for crystal stabilization, transmit carrier frequency stabilization and chip code timing

generation stabilization.

100. The system according to Claim 99, wherein said radio frequency transmit-only device includes a programming connecter through which said identification address, a type code, and a code division multiple access channel on which said RF transmit-only device is to operate are input in a serial data stream format.

101. The system according to Claim 99, wherein said random number generator is configured to be seeded with said identification address, thereby preventing repeat collisions.--

REMARKS

Favorable consideration of this application as presently amended is respectfully requested.

The present application is filed under Rule 53 and the present Preliminary Amendment amends the specification to refer to the related applications including co-pending parent application Serial No. 08/08/487,523 filed June 7, 1995 entitled Wireless Alarm System to which the present application claims priority.

The present Amendment adds new Claims 65-101 and cancels without prejudice Claims 1-64 which are being prosecuted in the parent application. Mr. H. Britton Sanderford and Mr. Robert E. Rouquette are the inventors of the invention defined by Claims 65-101, and thus, a Declaration will be filed by these two inventors at a later date. James D. Arthur, a named inventor in the parent case, is not an inventor of the invention defined by new Claims

65-101.

The present application is filed as a Rule 53 Continuation which permits an application to claim the benefit of a copending earlier filed application if the prior application is entitled to a filing date. Since the parent application Serial No. 08/487,523 is presently pending and is entitled to a filing date, the present claim for priority is considered proper, and consideration of the present application is earnestly solicited.

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(OSMMN 4/95)

UNITED STATES PATENT APPLICATION

of

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and

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for

WIRELESS ALARM SYSTEM

BACKGROUND OF THE INVENTION

This invention relates to a wireless warning system for use in a large office building, and more particularly a wireless fire warning and detection system which employs spread spectrum technology with high reliability for continuously monitoring the building.

DESCRIPTION OF THE PRIOR ART

A number of systems and techniques have been employed in the prior art as a warning system for large buildings. These include having warning sensors for detecting fire, security, or other means wired directly to a main console, with indicators that a particular sensor has been activated. Systems also have been developed employing a radio link between the sensor and receiver. For example, U.S. Patent No. 4,550,312 to Galloway et al. teaches the use of wideband sensors and transmitters. The sensors/transmitters transmit digital information to a central station by radio. These transmissions of messages are proceeded by an additional access code to identify a particular property. This increases the message overhead, however, which lowers system throughput and lowers battery life.

U.S. Patent No. 4,661,804 to Abel discloses a receiver-decoder used with a plurality of encode or transmitter

units using digitally encoded addresses. This use of multiple redundant 35 second interval short transmissions is used to achieve reliable throughput.

U.S. Patent No. 4,734,680 to Gehman et al. teaches the use of a pseudorandom number to lower probability of repeat data collisions. The Gehman invention provides for only four bits or sixteen time slot positions over which to transmit, which are inadequate for large systems with hundreds of transmitters. The Gehman disclosure does not teach the use of a randomization interval with hundreds of possible of time slots with spread spectrum so that a destructive data collision can only occur in one chip time. Further, the Gehman patent does not teach the use of the transmitters unique address as a seed to the pseudorandom number generator, preventing two transmitters from drifting into lockstep transmitting schedule.

OBJECTS AND SUMMARY OF THE INVENTION

An object of the present invention is to provide a wireless warning system having a high reliability for transmitting digital data via radio waves from an alarm or data transmission device to a remotely located receiver.

Another object of the invention is to provide a wireless warning system capable of data error detection and error correction using redundancy, for increasing communications

reliability.

A further object of the invention is to provide a wireless warning system having a safety margin against jamming and undesirable interference.

According to the present invention, as embodied and broadly described herein, a wireless warning system is provided comprising a plurality of sensors coupled to a plurality of spread spectrum transmitters, respectively. The plurality of sensors are for detecting or warning against smoke, heat, unauthorized entry, or other sensing device to indicate some particular function in a room of a building. The system further includes at least one spread spectrum receiver having polar diversity antennas and microprocessor having a display, with the microprocessor coupled to the spread spectrum receivers.

An apparatus coupled to a modulation input of an oscillator of a spread spectrum transmitter is provided for controlling the spread spectrum transmitter, which includes chip-code-generation means, preamble means, address means, and data means. The chip-code-generation means can be embodied as a recirculating register, the preamble means can be embodied as a preamble register, the address means can be embodied as an address register, and the data means can be embodied as a data register. The recirculating register is coupled to the modulation input of the oscillator for storing the spread spectrum code. The

recirculating register also outputs the spread spectrum chip code as a modulating voltage to the modulation input of the oscillator. The preamble register is coupled to the modulation input of the voltage controlled oscillator. The preamble register stores a preamble, and outputs, during a transmitting interval, the preamble as a modulating voltage to the modulation input of the voltage controlled oscillator. The preamble may include a coarse lock preamble and a fine lock preamble.

The address register is coupled to the modulation input of the voltage controlled oscillator through the preamble register. The address register stores a device address and a type code, and outputs, during a transmitting interval, the device address and the type code as a modulating voltage to the modulation input of the voltage controlled oscillator.

The data register is coupled to the data input and to the modulation input of the voltage controlled oscillator through the preamble register and the address register. The data register stores data received from the data input, and outputs, during the transmitting interval, the data as a modulating voltage to the modulation input of the voltage controlled oscillator.

The present invention further includes a error detection means coupled to the data register for putting a redundancy check code word at the end of a data sequence, for error detection.

A timing circuit is provided coupled to the enable input of

the voltage oscillator for enabling the voltage controlled oscillator during the transmitting interval. The timing circuit also is coupled to the keying input of the RF power amplifier for enabling an RF power amplifier during the transmitting interval. Additionally, a pseudorandom sequence generator is coupled to the timing circuit for generating a random number for modifying the timing duration between each transmitting interval.

The present invention also includes an apparatus for generation a spread spectrum chip code for use with a receiver, including means for entering the spread spectrum chip code having n single chips. The entering means may be embodied as a hand terminal. The apparatus further includes memory means for storing chip words, each chip word having a plurality of bits. The memory means may include a random access memory (RAM) or other memory device. Also included is a processing means coupled to the entering means and to the memory means, and responsive to receiving the spread spectrum chip code for transforming a single chip of the spread spectrum chip code to a chip word and storing the chip word in memory means. The processing means may be, for example, a microprocessor or other electronic circuit device to accomplish these functions. Additionally, counting means are included coupled to the memory means for sequencing through n addresses of the chip words stored in the memory means, and sequentially outputting the chip words to the receiver.

The present invention further includes an apparatus for synchronizing spread spectrum chip code using a two step algorithm in a process coupled to a receiver having a quieting output. The apparatus includes means for correlating a first signal from the quieting output of the receiver with ~~one chip~~ multiple code iterations of the spread spectrum chip code by comparing the first signal to an adaptive average to be exceeded by a preset margin. The means for correlating includes determining whether the amplitude of the first signal exceeds the preset margin. Included are means coupled to the correlating means for computing the adaptive average, in response to the first signal not exceeding the preset margin. The computing means adds the amplitude of the first signal to the previously computed adaptive average. Means coupled to the quieting output of the receiver is provided for correlating a second signal in response to the first signal exceeding the preset margin. The second signal is correlated with a portion the time duration of ~~one chip~~ multiple code iterations of the spread spectrum signal. The means for correlating the second signal compares the amplitude of the second signal to an adaptive average by a preset margin to determine whether the second signal exceeds the preset margin.

A second species of the spread spectrum chip code synchronization method and apparatus, according to the present invention, is provided. The second species includes the spread spectrum chip code synchronization apparatus coupled to a

baseband output of a receiver. The apparatus includes means coupled to the baseband output of the receiver for sampling and digitizing a plurality of analog signals from the baseband output of the receiver, for generating a plurality of data signals. Each of the analog baseband signals is sampled and digitized during one chip time. Register means are provided, coupled to the sampling and digitizing means, for shifting the plurality of data signals sequentially through a plurality of shift registers. Means is provided coupled to the register means for adding in parallel each of the plurality of data signals stored in the plurality of registers according to a plurality of predetermined weights for each of the plurality of data signals. The adding means generates a correlation sum.

Comparing means coupled to the adding means compares the correlation sum to a preset margin. Means coupled to the comparing means dithers a chip clock by at least one portion of one chip time, thereby improving clock lock.

A third species of the spread spectrum chip code synchronization apparatus is provided according to the present invention. The apparatus comprises means coupled to the baseband output of the receiver for sampling and digitizing a plurality of analog signals from the baseband output of the receiver. The sampling and digitizing means also generates a plurality of data signals. Each of the analog signals is sampled and digitized

during one chip time.

Register means also is provided in the third species of the spread spectrum chip code synchronization apparatus, according to the present invention, coupled to the sampling and digitizing means for shifting and recirculating the plurality of data signals sequentially through a plurality of shift registers. Means additionally is provided coupled to the register means for adding sequentially the data signals passing through one of the shift registers according to a predetermined weighting algorithm.

Additional objects and advantages of the inventions will be set forth in the description which follows, and in part will be obvious from the description, or may be learned by practice of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate a preferred embodiment of the invention, and together with the description, serve to explain the principles of the invention.

Fig. 1 is a block diagrammatic view of the wireless sensor and detector system according to the present invention;

Fig. 2 is a schematic diagram of a spread spectrum transmitter;

Fig. 3A is a block diagram of a spread spectrum receiver;

Fig. 3B is a schematic diagram of a spread spectrum chip code microprocessor of the receiver;

Fig. 4 is a flow chart of the code locking algorithm;

Fig. 5 is a timing diagram of the spread spectrum chip positions;

Fig. 6 is a schematic diagram of a parallel correlator coarse lock dither circuit for proving a fine lock; and

Fig. 7 is a schematic diagram of a parallel correlator with a serial correlation sum accumulation.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now be made to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings.

Wireless Warning Detection System

Fig. 1 illustrates the wireless warning system of the present invention. A plurality of sensors S1, S2, . . . , SN, are coupled to a plurality of spread spectrum transmitters X1, X2, . . . , XN, respectively. Also shown are the elements of a base station including a first spread spectrum receiver 502 and a second spread spectrum receiver 504, each of which are coupled to polar diversity antennas 507, 509, respectively. A microprocessor 506 having a microprocessor display is coupled to

the first spread spectrum receiver 502 and the second spread spectrum receiver 504. The wireless warning detection system of Fig. 1 provides a high reliability for transmitting digital data via radio waves from a sensor S1, S2, . . . , SN. The sensor S1, S2, . . . , SN may be, for example, a smoke head detector, a security sensing device, or other initiating device or modulating device. As set forth below, the high reliability of the system includes means for data error detection and error correction.

The preferred embodiment consists of many sensor devices S1, S2, . . . , SN which may be a smoke detector, pull station, contact alarm, waterflow detector, guard station, or security access controller. These can be expanded directly to include voice modulation, local area network data link, long-range alarm monitoring, remote power meter reading, remote process control, etc.

The initiating device provides either a contact input or reflected light smoke chamber level or data byte to the spread spectrum transmitters X1, X2, . . . , XN. The spread spectrum transmitters X1, X2, . . . , XN include means for data message encoding in serial form and data integrity validation, means for re-sending the message to achieve redundancy, means for randomizing the message transmit interval to avoid repeat collisions, means for modulating the serial message into spread spectrum form and means for transmitting the spread spectrum

carrier at the desired frequency.

The spread spectrum receiver's antennas 507, 509 minimize signal fading via polar diversity. Using two receivers provides redundancy as a primary and secondary means for receiving transmissions. The two polar diversity antennas provide spatial diversity against signal fading. The spread spectrum receiver 507, 509 collects the RF energy from polar diversity antenna 507, 509 and filters out undesirable frequencies. The receivers compare and synchronize desirable frequencies to the spread spectrum code of interest thereby extracting the original serial transmission. The spread spectrum receivers 507, 509 further validate the serial transmitter message and forward this information to computer 508 for display.

The spread spectrum of the present invention, in a preferred embodiment, uses fast frequency shift keying (FFSK). The techniques disclosed below are equally applicable for frequency hopping or phase shift keyed spread spectrum methods.

Transmitter

Referring to Fig. 2, a preferred embodiment of the transmitter of the instant invention is shown including chip-code-generation means, preamble means, address means, data means, timing means, pseudorandom-sequence means, and error-detection means. The chip-code-generation means may be

embodied as a recirculating register 10 and the preamble means may be embodied as a preamble register 11. The chip-code-generation means may be embodied as a shift register with exclusive ORed feedback taps. The address means may be embodied as an address register 14, the data means may be embodied as a data register 18, and the error-detection means may be embodied as cyclical-redundancy-check (CRC) generator 19. The timing means may be embodied as timing circuit 13, and the pseudorandom sequence means may be embodied as the random number generator 17.

In the exemplary arrangement shown, a microprocessor 8 includes the recirculating register 10, preamble register 11, address register 14, data register 18, CRC generator 19, random number generator 17, and timing circuit 13. The timing circuit 13 is embodied as a timing algorithm in software, located in microprocessor 8. Alternatively, these registers and circuits may be put together with discrete components or independently wired and constructed as separate elements, as is well known in the art.

As shown in Fig. 2, an oscillator, which is shown as a voltage controlled oscillator 2 is coupled to an RF power amplifier 3, and the RF power amplifier 3 is coupled through a bandpass filter 4 to a micropatch antenna 5. The voltage controlled oscillator 2 includes an enable input and a modulation

input, where the voltage controlled oscillator generates a spread spectrum signal in response to a modulating voltage being applied to the modulation input. The voltage controlled oscillator 2 is enabled by applying an enable signal to the enable input. The RF power amplifier 3 has a keying input and will amplify a signal from the voltage controlled oscillator 2 only if a keying signal is applied to the keying input. The voltage controlled oscillator 2 alternatively can be frequency locked to the microprocessor's crystal to improve stability. The voltage controlled oscillator 2 also can be replaced by a capacitor and inductor tuned oscillator and a phase shift keyed modulator, or any other means for generating a signal.

The microprocessor 8 is coupled to the modulation input of the voltage controlled oscillator 2 through first resistor R6 and second resistor R7. The microprocessor 8 broadly controls the voltage controlled oscillator 2 by supplying an enable signal to the enable input of the voltage controlled oscillator 2, and a modulating voltage to the modulation input of the voltage controlled oscillator 2. Also, the microprocessor 8 controls the RF power amplifier 3 by supplying a keying signal to the keying input of the RF power amplifier 3.

Included in the microprocessor 8 is a recirculating register 10 coupled to the modulation input of the voltage controlled oscillator 2 through second resistor R7. The recirculating

register 10 stores a spread spectrum chip code, and outputs, during a transmitting interval, the spread spectrum chip code as a modulating voltage to the modulation input of voltage controlled oscillator 2.

The preamble register 11 is coupled to the modulation input of the voltage controlled oscillator 2 through first resistor R6. The preamble includes the coarse lock preamble and the fine lock preamble. The preamble register 11 stores a coarse lock preamble in cells 12 and a fine lock preamble in cells 24. The preamble register 11 outputs during the transmitting interval, the coarse lock preamble and the fine lock preamble as a modulating voltage to the modulation input of the voltage controlled oscillator 2 through first resistor R6. First resistor R6 and second resistor R7 are chosen such that the desired spreading from the chip code and the data coming from the preamble register 11 is achieved.

Also shown in Fig. 2 is an address register 14 coupled to the modulation input of the voltage controlled oscillator 2 through the preamble register 11 and first resistor R6. The address register 14 stores a device address and a type code, and outputs during a transmitting interval, the device address and type code as a modulating voltage to the modulation input of the voltage controlled oscillator 2.

A data register 18 is coupled to a data input 20 and to the

modulation input of the voltage controlled oscillator 2 through the preamble register 14 and the address register 11. The data register 18 stores data received from the data input, and outputs, during the transmitting interval, the data as a modulating voltage to the modulation input of the voltage controlled oscillator 2. The data from the preamble register 11, address register 14, and data register 18 are outputted in sequence, and at the end of a sequence, the cyclical redundancy check generator 19 outputs a data word at the end of the code for error detection.

A timing circuit 13 is included in microprocessor 8, and is coupled to the enable input of the voltage controlled oscillator 2 and to the keying input of the RF power amplifier 3 for enabling the voltage controlled oscillator 2 and the RF power amplifier 3, by outputting an enable signal to the enable input and a keying signal to the keying input of the RF power amplifier 3, respectively, during the transmitting interval. In essence, voltage controlled oscillator 2 and RF power amplifier 3 are not active or activated during a time duration of non-transmission, and are only activate during a transmission interval. The time duration between transmission intervals is made to vary in response to the random number generator 17 generating a random number and transferring the random number to the timing circuit 13. The random number modifies the timing duration between each

transmitting interval randomly. ~~Alternatively, an algorithm based on the address of the facility having the spread spectrum transmitter, can be used with the facility address as the kernel for making the time between transmissions random.~~

Also shown are the voltage supply, regulator circuit 1, and battery low detector 25.

The spread spectrum transmitter monitors one or more data inputs 20 and transmits periodically a supervisory data message. One or more of the data inputs 20 can be set 21 such that they cause a priority transmission at an increased rate higher than the supervisory message rate.

During installation of the transmitter, a device address (1-4095) 12, "Type" code 15 (fire, security, panic, heat, pull station, etc.) stored in preamble register 11, and a spread spectrum chip code stored in recirculating register 10 are loaded via programming connector 16. At installation time the "Panel" computer assigns the device ID address to each room number or unique device in the system which is to be monitored. The panel computer then prints a sticky label with the device's ID, address, type code and spread spectrum chip code, both in decimal and bar code form. The label is fixed to the smoke detector or alarming device and via the programming connector 16, or the number can be entered manually with the aid of a hand-held terminal. Alternatively a bar code reader can be connected to

the programming connector 16 and the device can be read electronically from the bar code and entered into the transmitter. Microprocessor timing is controlled by crystal 23. Transmit timing is controlled by the wake-up timer 9, which has its own low power oscillator.

In operation, the transmitter sends a supervisory message often enough so that the receiver can detect failure of any transmitter within 200 seconds. The microprocessor 8 effectively "sleeps" between these transmissions to conserve battery life while counter 9 counts down to wake-up microprocessor 8. In order to minimize the chance of reoccurring data collisions from multiple simultaneous transmitters, the transmit interval is modified by random number generator 17. Very fine resolution intervals are used equal to ~~1000~~ 500 temporal transmit positions. The random number generator 17 is seeded with the transmitter's unique address 14, resulting in different transmit schedules for each unit, thereby avoiding continuous collisions between transmitters.

Once the microprocessor 8 is reset by the wake-up circuit 9 the timing circuit 13 allows the crystal 23 to stabilize for 1-5 ms. The timing circuit 13 then enables the transmitter oscillator 2 and allows it to stabilize for 1 ms. The timing circuit 13 subsequently enables the RF amplifier 3 by sending a

keying signal to the keying input. The RF energy from the RF amplifier 3 is filtered by bandpass filter 4 to reduce spurious RF emissions. The filtered signal is passed to a PCB foil micropatch 2 dBi gain antenna 5 which radiates the RF energy to an appropriate receiver. When the timing circuit 13 keys the RF power amplifier 3 it also begins to recirculate the spread spectrum 31 chip code stored in recirculating register 10 at a chip rate of 1 to 1.3 MHz. The chip code in turn causes a voltage swing 0-5 volts at the modulation input of the microprocessor. The voltage swing in conjunction with a modulation setting second resistor R7 creates a proportional current which modulates voltage controlled oscillator 2 thereby generating a spread spectrum FSK signal. ~~The modulator index of 90° causes the FSK signal to occupy an RF bandwidth of only 1.5 x chip rate.~~ This improves the signal to noise ratio at the receiver by reducing required bandwidth and minimizes the chances for intersecting interference. The data is super imposed on the chip code by the resistor 6 as a 1/31 deviation of the total modulation. Two or three adjacent chip code sequences are used to equal one bit time resulting in a baud rate of 14-21 KB/s.

In order for a receiver to demodulate a spread spectrum chip code, it must time lock onto the spread spectrum chip code. Disclosed are three methods of this timing acquisition, one is serial and two are parallel assisted. All methods require some

synchronization bits in the transmitted message specifically allocated to code timing acquisition, which allow the receiver to search the code and find a correlation peak. The serial correlator searches one bit time per chip in the code sequence to achieve a ±1/2 chip code lock. This search can be hastened by searching one code sequence time instead of one bit time thereby providing a two or three to one speed increase. The parallel correlator searches all 31 chip sequences in parallel so that an initial ±1/2 chip synchronization ("lock") can be achieved in one bit or one chip code sequence time. "Fine" code lock (±1/4 chip) for either serial or parallel assisted schemes must be followed by transmitted bit times allocated to allowing the receiver to achieve a higher resolution correlation "time" lock. One quarter chip lock accuracies perform to within ~~1.5 dB~~ 1.25 dB of optimal code alignment. The receiver's fine code lock algorithm seeks to optimize the correlation peak. Higher levels of code lock can be achieved by searching in smaller fractions of a chip. This can facilitate "time of flight" distance or location measurement applications such that 25 ns, 25 feet, of measurement resolution can be achieved.

The transmitter's microprocessor 8 stores a synchronizing preamble in preamble register 11 of 36 bits for a serial correlator, which are broken into 31 bits for coarse lock 11 and 5 bits for fine lock 12. For the two parallel correlation

methods disclosed 6 bits are used in the synchronizing preamble, 1 bit for coarse lock and 5 bits for fine lock. The actual code locking bits are transmitted as alternating ones and zeros so that the receiver's data demodulator can adaptively choose an optimal 1/0 voltage level decision point. The preamble is followed by a single data message synchronization bit 24 then 12 ID address bits 14 and 3 unit type bits 15 from address register 11, then 8 bits of input data from data register 18 and lastly 16 bits of CRC-16 data integrity check 19. The CRC-16 generator 19 is based on the entire proceeding message.

Once the message is transmitted, the timing circuit 13 turns off the enable signal at the enable input to voltage controlled oscillator 2 and the keying input of RF power amplifier 3, regenerates a new random number from random number generator 17, presets that number into the transmit interval wake-up circuit 9 and then sets the microprocessor 8 into the sleep mode. Battery voltage regulation is provided by a micropower regulator 1. Battery voltage is pulse tested to conserve battery life 25.

The CRC-16 generator can have its kernel seeded with an identification number unique to each facility. For example, the kernel can be set by the facility address. Any facility having a transmission system which uses such a unique code as the kernel for the CRC-16 generator can be separated ~~for~~ FROM ANY adjacent facilities without additional transmission time or message bits.

Receiver

The spread spectrum receiver comprises several major blocks:

A. The RF section which converts the received signal to lower frequencies;

B. Chip code generator with means of chip code phase shifting for correlation lock;

C. Means to measure both signal strength and quieting to detect correlation lock over the dynamic range of the system;

D. An adaptive data demodulator tolerant to DC i.e.: long strings of 1's or 0's; and

E. microprocessor algorithms to perform the above.

Fig. 3A shows the RF portion of the receiver which converts the received signal to lower frequencies. Fig. 3B shows a chip code generator with means for shifting a chip code phase for correlation lock, and means for measuring signal strength and the quieting output of the receiver to detect correlation lock over the dynamic range of the system. In Fig. 3A, a first polar diversity antenna 100 and a second polar diversity antenna 102 are shown and are physically turned so that their spatial phase relationship is 90^{o}. Signals received from each of the first and second polar diversity antennas 100, 102 are passed through a 45^{o} phase shifting network 104, 103, respectively and then to a

combiner 105. The combiner 105 combines the signals received from the first and second polar diversity antennas 100, 102. The combined signal then passes through a first bandpass filter 106, is amplified by amplifier 107 and passed through a second bandpass filter 108, and is mixed with the mixer 109. Typically, a crystal 125 controls the frequency of an oscillator 126. The signal from oscillator 126 is frequency multiplied by first, second and third frequency multipliers 128, 129, 130. The signal is mixed at first mixer 109 with the received signal from second bandpass filter 108. The oscillator 126 ~~receives~~ is modulated by the spread spectrum chip code through a phase shifter 127. The spread spectrum chip code is generated by the circuit in Fig. 3B. First mixer 109 down converts the received signal to a first intermediate frequency signal. The first intermediate frequency signal is in a first intermediate frequency range, and is passed through third bandpass filter 110, amplified by second amplifier 111 and passed through fourth bandpass filter 112. The output signal from bandpass filter 112 is mixed with a second mixer 113 with a second oscillator signal from second oscillator 132 to a second intermediate frequency. The frequency of the second oscillator 132 is controlled by second crystal 131 and frequency multiplied by fourth frequency multiplier 133. The second intermediate frequency signal is then passed through fifth bandpass filter 114, amplified by third amplifier 115, filtered

by sixth bandpass filter 116, and amplified by fourth amplifier 117. The second intermediate signal then passes via two routes. The first route passes through seventh bandpass filter 118, fifth amplifier 119 and quadrature detector 121. The quadrature detector 121 is coupled to a 90° phase shift network 120. The output of the quadrature detector 121 is the pre-data. Taps are taken from fourth and fifth amplifiers 117, 119. Signals from these taps pass through signal strength combiner 122, pass through eighth bandpass filter 123 and sixth amplifier 124. The output of sixth amplifier 124 is the signal strength.

Referring to Fig. 3B, an apparatus which is embodied as a microprocessor 147 is shown for synchronizing a spread spectrum chip code using a two step algorithm in a microprocessor coupled to the pre-data output of the receiver. The signal from the pre-data output of the receiver passes through circuitry for generating a quieting output of the receiver.

The signal from circuitry coupled to the pre-data output, for generating the quieting output, includes amplifier 135, ninth bandpass filter 140, signal compressor 141, quadrature detector filter 142 to produce the quieting output from seventh amplifier 143. The output of seventh amplifier 143 is the quieting output, and passes to the microprocessor 147 through analog to digital converter 150. The pre-data signal also passes through a filter comprising fourth and fifth resistors 138, 137 operational

amplifier 139 with sixth resistor 158, and first and second capacitors 157, 156. This signal is fed to the microprocessor 147.

The microprocessor 147 further includes means coupled to the correlation means for computing the adaptive average in response to the amplitude of the first data signal not exceeding the preset margin by adding the amplitude of the first data signal to the previously computed adaptive average. The microprocessor 147 comprises means coupled to the quieting output of the receiver via amplifier 143 for correlating the amplitude of a second data signal in response to the amplitude of the first data signal exceeding the preset margin. The second data signal is from the quieting output of the receiver. The first data signal is the digitized amplitude of the first signal, and the second data signal is the digitized amplitude of the second signal. When correlating the second data signal, the microprocessor 147 compares ~~a portion of one chip~~ multiple iterations of the spread spectrum chip code, by comparing the second data signal to the adaptive average by a preset margin to determine whether the amplitude of the second data signal exceeds the preset margin.

The microprocessor 147 synchronizes the spread spectrum chip code by comparing the first signal during one information bit to an adaptive average to determine whether coarse correlation has been achieved. In response to the first signal not achieving

coarse correlation, the microprocessor 147 computes an adaptive average by adding a first portion of the first data signal to a second portion of the adaptive average. Additionally, the microprocessor 147 correlates a second signal in response to the amplitude of the first signal exceeding the ~~quieting output of the receiver~~ + adaptive average by a preset margin within a portion of one chip of the spread spectrum chip code by comparing the amplitude of the second signal to the adaptive by a preset margin to determine whether the second signal exceeds the preset margin.

The microprocessor 147 also generates a spread spectrum chip code for use with the receiver, which is inputted through phase shifter 127 to oscillator 126 of Fig. 3A. The apparatus, which includes the microprocessor 147 and related circuitry, includes means for entering a spread spectrum chip code having n chips. The entering means may be embodied as hand terminal 153. Also, the apparatus includes memory means for storing chip words, which may be embodied as random access memory 146. The random access memory 146 is coupled to the microprocessor 147. The random access memory 146 stores each chip word having a plurality of bits per chip. In a preferred embodiment, there are four bits per chip word. The apparatus further includes counting means coupled to the random access memory 146 for sequencing through n addresses of the chip words in the random access memory 146 and sequentially outputting the chip words to the receiver. The

counting means may be embodied as adder 145 and timing circuit 147 with AND gate 159 for determining when to roll over when counting through n chip words. Clock divider 134 is included for controlling the microprocessor 147.

In operation, the RF energy is received by two polar diversity antennas 101 and 102 which are physically rotated 90 degrees, then phase shifted +45 degrees by the first phase shifter 103, and -45 degrees by the second phase shifter 104 and finally summed 105. This polar diversity method enhances faded area reception. The signal is bandwidth limited to 2.0 MHz by a first bandpass filter 106, amplified by first amplifier 107 and bandpass filtered by second bandpass filter 108 before being presented to the first mixer 109.

The first local oscillator generated by a crystal controlled oscillator 126 which is then phase modulated to the equivalent frequency pull of a modulation of 90^{o} at a rate set by the chip code generator.

The chip code is initially selected by either the hand terminal 153 or by the remote serial port 155. Four chip code sets are loaded into the RAM 146 such that a single "1" is represented as "1111", this allows sub chip code searches by sequencing the two low order ram address bits. The ram memory is addressed at four times the chip rate so that 1/4 chip resolution code searches can be performed. The counter 144 in conjunction

with the clock input 156 sets this chip code rate. The binary counter 144 causes the RAM 146 to sequentially select and modulo repeat the entire stored chip code. The AND gate 59 determines the 31st count state x 4 to create a reset pulse and causes the counter to cycle through (31 x 4) modulo states. In order to rapidly jump to any chip code table position the summer 145 is used to add offset 161 selected by the microprocessor's search algorithm. The flip-flop 160 synchronizes the output of the RAM 146 to the chip code clock 156 to avoid variable propagation delays due to the counters and adders.

Once the chip code has modulated the oscillator 126, the combined signal is multiplied by 128, 129, and 130 to provide a signal from the first local oscillator to frequency mixer 109. This mixing stage 109 provides several features including lowering the frequency to 160 MHz, narrowing the bandwidth to 125 kHz, and when the microprocessor locks the code sequence, the mixer 109 despreads the original transmitted data signal.

The first mixer 109 output is bandpass filtered by third bandpass filter 110, amplified by second amplifier 111 and bandpass filtered by fourth bandpass filter 112. The first intermediate frequency signal is mixed by second mixer 13 with a signal from the second local oscillator. The second local oscillator signal originates from second oscillator 132 and is controlled by crystal 131. The resulting sine wave is frequency

multiplied by fourth frequency multiplier 133 before being mixed at second mixer 113. The signal resulting from the second mixer 113 is lowered in frequency to 10.7 MHz and is bandpass filtered by fifth bandpass filter 114, amplified by third amplifier 115 and bandpass filtered by sixth bandpass filter 116. This signal is sent to fourth amplifier 117 with feedback bias current measured along with fifth amplifier 119 by a signal strength measurement circuit 122. The signal strength measurement is low pass filtered by first lowpass filter 123 and buffered by sixth amplifier 124 before passing to the signal strength analog multiplexer input 152.

The signal from fourth amplifier 117 is filtered by sixth bandpass filter 118 and amplified by fifth amplifier 119. This output of fifth amplifier 119 is then quadrature detected with the aid of phase shifting circuit 120. The output of the quadrature detector 121 is buffered by amplifier 135, then high pass filtered 140. The signal is compressed to a manageable 45 dB dynamic range by compressor 141. The compressed signal is passed through a quieting detector filter 142 and buffered by amplifier 143 before being inputted to the analog multiplexer input 151.

The "pre-data", buffered by amplifier 135, is also presented to an adaptive data demodulator. Varying DC levels will be present on this signal due to frequency uncertainty between the

receiver and transmitters. The data 1/0 decision threshold is chosen as the average voltage of an alternating 1/0/1... pattern in the synch preamble. During the preamble code lock search time, the analog switch 136 is enabled and pre charges capacitor 156 through resistor 137. This places an average voltage on capacitor 156 between a logic "1" and a logic "0". Once code lock is achieved, and the data message synchronization bit 24 is detected, the analog switch 136 is opened leaving the capacitor 156 at a stable level for the duration of the message. The buffered pre-data level is then filtered 157 with hysteresis set by resistors 158 and 138 and compared to the voltage level on capacitor 156. This results in reliable data bits provided on the output of voltage comparator 139.

Code Locking Algorithm

The code locking algorithm seeks to determine a correlation peak by comparing the received RF signal energy to a microprocessor controlled copy of the desired chip code pattern. The code locking algorithm digitizes the quieting detectors analog output once per bit time. The software maintains an adaptive average of the quieting samples to determine the level of correlation improvement. The described algorithm code locks to within 1/4 chip time or within 1.25 dB of optimum. The ~~signal strength or~~ baseband output also can be used in place of the

quieting output.

The present invention includes three methods of using a microprocessor for synchronizing the timing acquisition of a spread spectrum chip code received by the receiver. The spread spectrum signal comprises a plurality of information bits. Each information bit is spread in spectrum by a plurality of chips from a spread spectrum code. The first method, as depicted in Fig. 4, comprises the steps performed by the microprocessor of inserting 401 a delay of one information bit time before the first information bit received by the receiver, and sampling and digitizing 402 the first signal from the quieting output of the receiver to generate a first data signal. The sampling and digitizing alternatively can be taken from the baseband or signal strength output of the receiver. The first method compares 404 the amplitude of the first data signal to the adaptive average during the time of one information bit to determine whether coarse correlation has been achieved. In response to coarse correlation not being achieved, the method computes 405 the adaptive average by adding a first portion of the amplitude of the first data signal to a second portion of the previously computed adaptive average. If the coarse correlation has been achieved, then the method shifts 407 the chip code by a third portion of one information bit time. In a preferred embodiment of the present invention, the chip time is divided into four

portions, thus the shifts 407 is equivalent to delaying the chip by 1/4 chip time duration.

An additional delay is inserted 408 and the method samples and digitizes 409 a second signal from the quieting output of the receiver to generate a second data signal. The amplitude of the second data signal during one information bit time is compared 410 to the adaptive average to determine whether fine correlation has been achieved. If fine correlation has been achieved, then a data capture algorithm is initiated 414. If fine correlation has not been achieved, then the method shifts 412 the chip code phase shifter by a third portion, which is equivalent in the present preferred embodiment to a 1/4 time duration of a chip. The method then proceeds to initiate the data capture algorithm.

A delay 401 is inserted before digital conversion of the quieting output 402. This delay serves to insure re- occurring data samples equal to one information bit time. The new sample is compared to the running adaptive average 403. If the improvement is greater than a preset margin, then coarse correlation 404 is achieved. Otherwise, if the new sample is within the noise error of the running average, the new sample is combined with the old average 405; average = (.25 new + .75 old average). The chip code phase shifter 161 is incremented by a count of 4 (1 chip time). This coarse code lock algorithm is then indefinitely repeated until coarse code lock is acquired.

If coarse correlation is achieved 404, then the algorithm seeks to "fine" code lock. The chip code phase shifter 161 is shifted 407 by one (1/4 chip time). The one information bit time synchronizing delay is passed 408. The quieting detector output is digitized 409 and compared 410 to the running quieting output average. If the new sample did not improve 411 the quieting by the preset margin then the chip code phase shifter is incremented 412 by 1/4 chip to its past more optimum position. Fine lock is completed 414 and the code lock algorithm jumps to a data capture algorithm.

If the required margin of quieting improvement is achieved 411, then the number of chip code shifts is checked 413. Any search code position which is shifted more than three 1/4 chip steps would undesirably slip one whole code cycle. Comparison 413 stops a search on the third-code slip and assumes an optimum correlation is achieved then proceeds to the data acquisition algorithm 414. If three code phase decrements have not occurred, the algorithm repeats at shift 407.

Fig. 5 shows four cases with one-quarter chip code lock achieved in each case using the first method.

A second method and apparatus for synchronizing a spread spectrum chip code using the baseband signal output of the receiver is shown in Fig. 6. The apparatus aspect of the invention includes means for sampling and digitizing a plurality

of analog baseband signals, register means for shifting the plurality of data signals, means for adding in parallel the plurality of data signals, means for comparing the correlation sum and means for dithering a chip/sample clock by a portion of a chip time. The sampling and digitizing means may be embodied as analog to digital converter 201 The register means may be embodied as the plurality of registers 202, 203, 204. The adding means may be embodied as adders 205, 206, 207 and the comparing means may be embodied as comparator 213. The dithering means may be embodied as the microprocessor 215.

As illustratively shown, the apparatus for synchronizing the spread spectrum chip code has the analog to digital converter 201 coupled to the RF baseband output of the receiver 212. The analog to digital converter 201 samples and digitizes the plurality of analog baseband signals from the baseband output of the receiver 212 and generates a plurality of data signals. The plurality of registers 202, 203, 204 is coupled to the analog to digital converter 201 and shifts the plurality of data signals sequentially through the plurality of registers 202, 203, 204. The plurality of adders 205, 206, 207 are coupled to the plurality of registers 202, 203, 204, respectively, for adding in parallel each of the data signals stored in the plurality of registers 202, 203, 204 according to a plurality of predetermined weights for each of the plurality of data signals, respectively,

to generate a correlation sum. The weights are controlled by flip flop circuits 209, 210, 211, which contain the spread spectrum chip code. The adder 207 outputs a correlation sum 208 to a comparator 213 for comparing the correlation sum to a predetermined margin or threshold. The dithering circuit embodies as a microprocessor 215 is coupled to the comparator 213 and dithers the chip clock by at least a first portion of one chip time, thereby improving chip lock.

In operation, the second method of using a microprocessor for synchronizing the timing acquisition of the spread spectrum chip code received by a receiver comprises the steps of sampling and digitizing using the analog to digital converter 201, the plurality of analog baseband signals from the baseband output of the receiver 212, to generate a plurality of data signals. Each of the analog baseband signals is sampled and digitized during one chip time. The method shifts the plurality of baseband signals through the plurality of shift registers 202, 203, 204. The plurality of data signals are added in parallel according to a plurality of predetermined weights, from flip flops 209, 210, 211 for each of the plurality of data signals, respectively, in the plurality of adders 205, 206, 207 to generate a correlation sum 208. The correlation sum 208 is compared to a predetermined threshold or preset margin, and a chip clock is then dithered by at least a first portion of one chip time to improve clock lock.

In a preferred embodiment, the first portion is one quarter of one chip time.

The chip clock samples once per chip time. A coarse chip lock may therefore be incorrect by ±1/2 of a chip. To improve the lock, the chip clock is slewed in ±1/4 and/or ±1/8 chip steps controlled by an algorithm in microprocessor 215. A clock with a rate equal to four times the chip rate is counted by counter 214. The counters output is compared to an output of the microprocessor 215 equal to the code phase being searched. The microprocessor 215 can thereby search in fine chip code steps after a rapid parallel assisted search in 1, 31 chip code time. The total search required is equal to 6 chip code times, which can be sent in the spread spectrum transmitters code-lock preamble as disclosed.

As a further component reduction of the circuitry described above in the second species of the method and apparatus for synchronizing a spread spectrum chip code, the parallel assisted chip code lock can be serially summed instead of parallel summed. The serial sum of all 31 stages must be computed between chip samples (less than 1,000 ns). This speed can be achieved with available high speed CMOS ASICS with clock speeds of 40 MHz or greater.

A third species of the spread spectrum chip code synchronizing method and apparatus is disclosed in the present

invention, and is set forth in Fig. 7. The third species of the spread spectrum chip code synchronizing apparatus couples to the baseband output of the receiver. The apparatus includes means coupled to the baseband output of the receiver for sampling and digitizing the plurality of analog baseband signals, register means coupled to the sampling and digitizing means for shifting and recirculating the plurality of data signals, and means coupled to the register means for adding sequentially the data signals passing through the shift register means. As shown in Fig. 7, the sampling and digitizing may be embodied as analog to digital converter 310. The register means may be embodied as registers 307, 308, 309 and the adding means may be embodied as adder 303. As shown in Fig. 7, the analog to digital converter 310 is coupled to the baseband output of the receiver, and passes through a plurality of gates 302 to the plurality of registers 307, 308, 309, to adder 303. Also shown is a plurality of flip flops 306, 311, 312 having the spread spectrum chip code therein. The flip flops 306, 311, 312 input the spread spectrum chip code into the adder 303. The adder 330 is coupled to a correlation sum accumulator 304 which outputs a correlation sum 305.

In the preferred embodiment, the third species of the apparatus for synchronizing the spread spectrum chip code has the analog to digital converter 310 coupled to the baseband output of

the receiver for sampling and digitizing a plurality of analog baseband signals and generating a plurality of data signals. Each of the analog baseband signals is sampled and digitized during one chip time. The plurality of registers 307, 308, 309 is coupled to the analog to digital converter 310 through gates 302 for shifting and recirculating the plurality of data signals sequentially through the plurality of registers 307, 308, 309 and gates 302. The adder 303 is coupled to register 309 for adding sequentially the data signals passing through registers 309 according to predetermined weights set forth in flip flops 306, 311, 312.

In operation, the third method of uses a microprocessor for synchronizing the timing acquisition of the spread spectrum chip code received by the receiver. The method samples and digitizes the plurality of analog baseband signals from the baseband output of the receiver using analog to digital converter 310, to generate a plurality of data signals. Each of the analog baseband signals is sampled and digitized during one chip time. The method further includes shifting and recirculating the plurality of data signals sequentially through the plurality of registers 307, 308, 309. The data signals are added sequentially as they pass through register 309 using adder 310 and accumulated. The correlation sum accumulator 304 then passes the correlation sum 305 to the microprocessor.

The third method is similar to the second method, except that there is only one adder 303 for the entire register chain instead of one adder per stage. The registers 307, 308, 309 are steered to recirculated by the AND/OR gates 302. The stored chip code string can also be shifted and recirculated. After each chip clock rising stage transition, an analog data sample is converted by analog to digital converter 310 and stored in register 307. Data in the registers are shifted to the right as in the circuit in of Fig. 6. Immediately following the chip sample, a sequence is performed to accumulate a correlation sum. The AND/OR steering gates 301 and 302 are switched to the "sum" state. This passes a high speed summing clock of 40 MHz for 31 clock cycles to the registers 307, 305, 309 and to the stored spread spectrum chip code in 306, 311, 312. The steering gates 302 causes data in registers 307, 305, 309 to recirculate so that after 31 clock cycles of the adding phase, the data in registers 307, 308, 309 will be in their original positions and ready to accept another spread spectrum chip code data sample and store phase. After each 40 MHz summing clock transition a new sum is generated by adder 303 and accumulated in accumulator 304. Adder 303 is caused to either add or subtract the inputs Ain from the accumulated total. This is determined by the stored chip code string in flip-flop 312 which creates the x (+1) or x (-1) correlation weighting causing either the addition or subtraction

of the Ain inputs. The outputs of accumulator 304 are transferred to the next register stage and then at the next clock rising edge, the accumulator stores that total. After 31 summing clock cycles the accumulation 304 will contain the correlation sum 305. The multibit words stored and summed by the two alternative methods can be reduced to one bit samples and sums, resulting in a small loss of performance.

It will be apparent to those skilled in the art that various modifications can be made to the wireless detection system of the instant invention without departing from the spirit or scope of the invention, and it is intended that the present invention cover modifications and variations of the wireless detection system provided they come within the scope of the appended claims and their equivalents.

WHAT IS CLAIMED AS NEW AND DESIRED TO BE SECURED BY LETTERS PATENT OF THE UNITED STATES IS:

1. In a method for controlling a spread spectrum transmitter having an oscillator provided with a modulation input, the improvement comprising:

maintaining the transmitter in a low current state between transmissions of spread spectrum signals;

generating one or more chip code sequence repetitions during a transmitting interval when the transmitter is not maintained in the low current state and applying the generated chip code sequence repetition as a modulating voltage to the modulation input of the oscillator thereby causing a frequency deviation in the transmitter output;

applying a device address and data to the modulation input of the oscillator after modulating the oscillator with the chip code sequence repetition for a predetermined time period such that the modulation index of the transmitter during application of the address device and the data is less than that of the modulation index of the transmitter during application of only the chip code sequence.

2. The method of claim 1, further comprising:

limiting the number of address and data bits applied to the modulation input of the oscillator so that an associated receiver which receives the transmitted signal can successfully decode the transmitted data after completion of coarse search and without the use of continuous chip code synchronization by the receiver.

3. The method of claim 1, further comprising:

applying the generated chip code sequence repetition to the oscillator at a chip rate of approximately 1.0-1.3 Mc/s to produce a frequency shift keying (FSK) spread spectrum modulated signal.

4. The method of claim 1, wherein said oscillator comprises a tuned oscillator and a phase shift keying modulator, further comprising:

applying the generated chip code sequence repetition to the phase shift key modulator at a chip rate of approximately 1.0-1.3 Mc/s to produce a phase shift keying (PSK) spread spectrum modulated signal.

5. A spread spectrum chip code synchronization method for synchronizing a spread spectrum signal received by a receiver having an output, comprising the following steps:

causing a receiver chip code generator to sequentially advance or delay in time a chip code generated by the generator;

correlating a first signal received by the receiver within one chip time alignment of the chip code generated by the generator by comparing the first signal to an adaptive average to determine whether the first signal exceeds the adaptive margin by a preset margin;

updating the adaptive average by adding a portion of the first signal to a portion of the adaptive average used during correlating of said first signal to produce a new adaptive average;

ceasing the sequential advance or delay of the chip code generated by the chip code generator when, during the correlating

step, it is determined that the first signal exceeds the adaptive average by said preset margin, thereby achieving initial chip code synchronization operation; and

decoding data provided at a receiver output.

6. The method of Claim 5, comprising:

decoding said data without continuous receiver chip code generator re-synchronization.

7. A spread spectrum chip code synchronization method for synchronizing a spread spectrum signal received by a receiver having an output, comprising the following steps:

causing a receiver chip code generator to sequentially advance or delay in time a chip code generated by the generator;

correlating a first signal received by the receiver within one chip time alignment of the chip code generated by the generator by comparing the first signal to an adaptive average to determine whether the first signal exceeds the adaptive average by a preset margin;

updating the adaptive average by adding a portion of the first signal to a portion of the adaptive average used during correlating of said first signal to produce a new adaptive average;

correlating a second signal received by the receiver in response to a determination in the step of correlating the first signal that the first signal exceeds the adaptive margin by said preset margin, within a portion of one chip time alignment of the spread spectrum chip code, by comparing the second signal to the new adaptive average to determine if there is a correlation improvement;

adjusting the chip code position of the chip code generator by a portion of a chip time in dependence on whether or not there was an improvement in correlation in the preceding step of correlating the second signal; and

decoding data provided at an output of the receiver.

8. The method of claim 7, comprising:

decoding data while chip code synchronization within the receiver runs open loop.

9. A spread spectrum transmitter comprising:

oscillator means having a modulation input and producing a variable frequency output tuned to a carrier frequency to be transmitted;

a chip code generator coupled to the modulation input of the oscillator means to change the frequency of the output of the oscillator means to produce a spread spectrum frequency shift keying (FSK) modulated signal at said carrier frequency;

a buffer amplifier coupled to the output of the oscillator means to amplify the spread spectrum FSK modulated signal at said carrier frequency;

a filter coupled to an output of the buffer amplifier to filter the amplified spread spectrum FSK modulated signal at said carrier frequency; and,

an antenna coupled to an output of the filter for transmitting the amplified and filtered spread spectrum FSK modulated signal at said carrier frequency.

10. The transmitter of claim 9, comprising:

a crystal oscillator for applying a clock signal to said chip code generator; and

means for locking the oscillator means to the clock produced by said crystal oscillator.

11. The transmitter of claim 10, comprising:

said chip code generator being clocked at a chip rate of approximately 1.0 - 1.3 Mc/s.

12. The spread spectrum transmitter according to claim 9, further comprising:

a data storage device coupled to the modulation input of the oscillator means for applying to said modulation input data bits having an amplitude such that a frequency change produced in the transmitter carrier frequency by the oscillator means is less broad than that of a frequency change produced in the transmitter carrier frequency when only a chip code from the chip code generator is applied to the modulation input of the oscillator means, thereby simultaneously producing FSK data modulation and FSK spreading modulation at a desired carrier frequency.

13. The spread spectrum transmitter of claim 12, further comprising:

timer means for causing the chip code generator to produce one or more chip code sequences applied to the modulation input of the oscillator means for a predetermined time period, for the purpose of spread spectrum synchronization at a receiver, prior to the data storage device outputting sequential data bits to the modulation input of the oscillator means.

14. The spread spectrum transmitter according to claim 12, further comprising:

first timer means for applying for a predetermined time period to the modulation input of the oscillator means, for the

purpose of spread spectrum synchronization at a receiver, a chip code produced by the chip code generator and having one or more chip code sequences and an amplitude and pattern so that a data detector in the receiver is precharged in order to overcome system tolerances between the transmitter and the receiver; and

second timer means to produce a predetermined delay in application of data from the data storage device to the modulation input of the oscillator means after application of only said chip code of one or more chip code sequences.

15. A spread spectrum transmitter according to claims 9, 12, 13 or 14, further comprising:

frequency stabilization means for reducing a frequency offset error at the oscillator means.

16. A spread spectrum transmitter according to claims 9, 10, 11, 12, 13 or 14, wherein said oscillator means includes an enable input and the buffer amplifier includes an enable input, comprising:

control means connected to the enable input of the oscillator means and the enable input of the buffer amplifier for enabling said oscillator means and said buffer amplifier only during transmission from the transmitter thereby to reduce power drain and ensure adequate settling time.

17. A spread spectrum transmitter according to claims 9, 12, 13 or 14, further comprising:

modulation index setting means for setting a frequency deviation of the oscillator means in response to modulating signals applied to the modulation input of the oscillator means to generate fast frequency shift keying (FFSK) transmissions.

18. A spread spectrum transmitter according to claims 9, 12, 13 or 14, further comprising:

an address storage device for storing addresses;

error detection generation means for detecting errors in data to be transmitted; and

means for applying addresses stored in the address storage device and error detection signals generated by the error detection generation means to the modulation input of the oscillator means at an amplitude less than the amplitude of the chip code applied to the modulation of the input by the chip code generator, thereby sequentially modulating the output frequency of the oscillator means less broadly than when the chip code alone is applied to the modulation input of the oscillator means.

19. A spread spectrum transmitter according to claims 9, 12, 13 or 14, further comprising:

means for limiting a length of a data message transmitted so that once initial spread spectrum synchronization is achieved by a receiver, a receiver can run open loop without performing ongoing chip code resynchronization.

20. A spread spectrum transmitter comprising:

oscillator means having a modulation input and producing a variable frequency output;

a chip code generator coupled to the modulation input of the oscillator means to change the frequency of the output of the oscillator means to produce a spread spectrum frequency shift keying (FSK) modulated signal;

multiplication means for multiplying the frequency output of the oscillator means by a predetermined integer multiple of

the frequency of the oscillator means to produce a desired carrier frequency;

a buffer amplifier coupled to the output of the multiplication means to amplify the frequency multiplied spread spectrum FSK modulated signal and produce a corresponding signal at an output of the buffer amplifier;

a filter coupled to the output of the buffer amplifier to filter the output of the buffer amplifier; and,

an antenna coupled to an output of the filter for transmitting the amplified and filtered spread spectrum FSK modulated signal at said carrier frequency.

21. A spread spectrum transmitter comprising:

a voltage controlled oscillator (VCO) having a modulation input and a frequency output tuned to a desired carrier frequency;

a chip code generator coupled to the modulation input of the VCO to apply a chip code sequence to the modulation input and thereby modulate the frequency output of the VCO to generate a spread spectrum signal; and

data storage means coupled to the modulation input of the VCO to apply data stored in the data storage device to the modulation input of the VCO at a level which produces less broad modulation of the frequency output of the VCO than when only the chip code sequence is applied to the modulation input, thereby simultaneously producing a fast frequency shift keying (FFSK) data signal.

22. The spread spectrum transmitter according to claim 21, further comprising:

frequency stabilization means for reducing offset error in the frequency of the output of the VCO.

23. The spread spectrum transmitter according to claim 21, further comprising:

a buffer amplifier for amplifying the frequency output of the VCO;

said VCO and said buffer amplifier each having an enable input;

control means connected to the enable input of the VCO and the enable input of the buffer amplifier for enabling said VCO and said buffer amplifier only during transmission from the transmitter thereby to reduce power drain and ensure adequate settling time.

24. The spread spectrum transmitter according to claim 22, further comprising:

modulation index setting means for setting a frequency deviation of the VCO in response to modulating signals applied to the modulation input of the VCO to generate fast frequency shift keying (FFSK) in order to minimize transmitted band width.

25. A spread spectrum transmitter according to claim 24, further comprising:

an address storage device for storing addresses;

error detection generation means for detecting error in data to be transmitted; and

means for applying addresses stored in the address storage device and error detection signals generated by the error

detection generation means to the modulation input of the VCO at an amplitude less than the amplitude of the chip code applied to the modulation of the input by the chip code generator, thereby sequentially modulating the output frequency of the VCO less broadly than when the chip code alone is applied to the modulation input of the VCO.

26. The spread spectrum transmitter according to claim 25, further comprising:

multiplication means for multiplying the frequency output of the voltage controlled oscillator by a predetermined integer multiple of the frequency of the VCO to produce a desired carrier frequency.

27. The spread spectrum transmitter according to claims 26, further comprising:

means for limiting a length of a data message transmitted so that once initial spread spectrum synchronization is achieved by a receiver, a receiver can run open loop without performing chip code synchronization.

28. A spread spectrum transmitter comprising:

oscillator means having an output set to a carrier frequency;

a phase shift key modulator having an input coupled to the output of the oscillator means and having a modulation input;

a chip code generator connected to the modulation input of the phase shift key modulator to apply a chip code sequence to the modulation input of the phase shift key modulator and thereby produce a phase shift key spread spectrum modulated signal at the

said carrier frequency at an output of said phase shift key modulator;

a buffer amplifier having an input coupled to an output of the phase shift key modulator;

a filter having an input coupled to an output of the buffer amplifier; and

an antenna having an input coupled to an output of the filter to transmit the amplified and filtered phase shift key spread spectrum modulated signal at the carrier frequency;

timer means for applying one or more chip code sequences to the modulation input of the phase shift key modulator prior to transmission of data thereby to promote spread spectrum synchronization in a receiver receiving a spread spectrum modulated signal transmitted by the antenna;

address storage means for storing addresses;

data means for storing data; and

error detection generation means for providing error detection bits to secure the data to be transmitted.

29. The spread spectrum transmitter of claim 28, further comprising:

means for applying addresses stored in the address storage means, data stored in the data means, and error detection signals generated by the error detection generation means to the modulation input of the phase shift key modulator, thereby sequentially outputting address, data and error detection code.

30. The spread spectrum transmitter according to claims 28 or 29, further comprising:

frequency stabilization means for reducing frequency offset error at the output of the VCO.

31. The spread spectrum transmitter according to claims 28 or 29, further comprising:

said oscillator means and said buffer amplifier each having an enable input; and

control means connected to the enable input of the oscillator means and the enable input of the buffer amplifier for enabling said oscillator means and said buffer amplifier only during transmission from the transmitter thereby to reduce power drain and ensure adequate settling time.

32. A spread spectrum transmitter comprising:

carrier frequency generation means for generating a carrier frequency at an output;

frequency stabilization means for reducing frequency offset error at the output of the oscillator means;

a phase shift key modulator having an input coupled to the output of the means and having a modulation input;

a chip code generator connected to the modulation input of the phase shift key modulator to apply a chip code sequence to the modulation input of the phase shift key modulator and thereby produce a phase shift key spread spectrum modulated signal at the frequency of the carrier frequency generation means at an output of said phase shift key modulator;

multiplication means for multiplying the output of the phase shift key modulator by a predetermined integer multiple of the

frequency of the carrier frequency generation means to produce a desired transmitted frequency;

a buffer amplifier having an input coupled to an output of the multiplication means;

a filter having an input coupled to an output of the buffer amplifier; and

an antenna having an input coupled to an output of the filter to transmit the multiplied, amplified and filtered phase shift key spread spectrum modulated signal at said desired transmitted frequency;

timer means for controlling application from said chip code generator of one or more chip code sequences to the modulation input of the phase shift key modulator prior to transmission of data thereby to promote spread spectrum synchronization in a receiver receiving a spread spectrum modulated signal transmitted by the antenna;

address storage means for storing addresses;

data means for storing data;

error detection generation means for providing error detection bits to secure the data to be transmitted; and

means for applying addresses stored in the address storage means, data stored in the data means, and error detection signals generated by the error detection generation means to the modulation input of the phase shift key modulator, thereby sequentially outputting address, data and error detection code.

33. The spread spectrum transmitter according to claims 28, 29, 30, 31 or 32, further comprising:

means for limiting a length of a data message transmitted so that once initial spread spectrum synchronization is achieved by a receiver, the receiver can run open loop without performing ongoing chip code resynchronization.

34. A spread spectrum transmitter comprising:

oscillator means, including a voltage controlled oscillator having a modulation input, for generating a transmitter output at a carrier frequency;

processor means for controlling transmissions by the voltage controlled oscillator, said processor means including processor oscillator means for producing a frequency stabilizing reference clock signal;

means for stabilizing the frequency of the voltage controlled oscillator by locking the frequency of the voltage controlled oscillator to the frequency stabilizing reference clock signal produced by said processor oscillator means;

timer means for defining an active operating state in which the processor means and the voltage controlled oscillator are enabled, said timer means first enabling said processor oscillator means for a predetermined time to stabilize the frequency output of the processor oscillator means and thereafter enabling said voltage controlled oscillator for a predetermined time to allow the frequency output of the voltage controlled oscillator to stabilize, said timer means also defining an inactive state in which the processor means is not enabled and

the voltage controlled oscillator is not enabled and no carrier frequency at the transmitter output is produced; and

said processor means further comprising chip code generator means clocked by the processor oscillator means for generating a chip code signal applied to the oscillator means, thereby locking the transmitter carrier frequency to the processor reference clock signal.

35. The transmitter of Claim 34, wherein said oscillator means comprises:

phase shift keying means connected to the output of the voltage controlled oscillator and having a modulation input to which is applied the chip code signal, thereby producing a spread spectrum phase shift key signal at said carrier frequency.

36. The transmitter of Claim 34, further comprising:

means for applying the chip code signal to the modulation input of the voltage controlled oscillator so that at the output of the voltage controlled oscillator there is produced a frequency shift keyed spread spectrum signal at said carrier frequency.

37. The transmitter of Claims 1, 9, 21, 28, 32, 34 or 35, further comprising:

means for generating plural transmit messages applied to said oscillator means for transmission by the transmitter, thereby to provide message redundancy.

38. The transmitter of Claim 37, wherein said means for generating plural transmit messages comprises:

means for generating said plural messages with different time intervals therebetween to provide message redundancy with

a lowered probability of repeat collision in the presence of multiple transmitters.

39. The spread spectrum transmitter according to claims 34, 35, or 36, further comprising:

said voltage controlled oscillator having an enable input;

a buffer amplifier, having an enable input, for amplifying the output of the voltage controlled oscillator; and,

control means connected to the enable input of the voltage controlled oscillator and the enable input of the buffer amplifier for enabling said voltage controlled oscillator and said buffer amplifier only during a transmission from the transmitter thereby to reduce power drain and ensure adequate settling time.

40. The spread spectrum transmitter according to claim 37, further comprising:

said voltage controlled oscillator having an enable input;

a buffer amplifier, having an enable input, for amplifying the output of the voltage controlled oscillator; and,

control means connected to the enable input of the voltage controlled oscillator and the enable input of the buffer amplifier for enabling said voltage controlled oscillator and said buffer amplifier only during a transmission from the transmitter thereby to reduce power drain and ensure adequate settling time.

41. The spread spectrum transmitter according to claims 34, 35 or 36, further comprising:

modulation index setting means for setting a frequency deviation of the voltage controlled oscillator in response to

modulating signals applied to the modulation input of the VCO to generate fast frequency shift keying (FFSK) in order to minimize transmitted bandwidth.

42. The spread spectrum transmitter according to claim 37, further comprising:

modulation index setting means for setting a frequency deviation of the voltage controlled oscillator in response to modulating signals applied to the modulation input of the VCO to generate fast frequency shift keying (FFSK) in order to minimize transmitted bandwidth.

43. A spread spectrum transmitter according to claims 34, 35 or 36, further comprising:

an address storage device for storing addresses;

error detection generation means for detecting error in data to be transmitted; and

means for applying addresses stored in the address storage device and error detection signals generated by the error detection generation means to the modulation input of the VCO at an amplitude less than the amplitude of the chip code applied to the modulation of the input by the chip code generator, thereby sequentially modulating the output frequency of the voltage controlled oscillator less broadly than when the chip code alone is applied to the modulation input of the voltage controlled oscillator.

44. A spread spectrum transmitter according to claim 37, further comprising:

an address storage device for storing addresses;

error detection generation means for detecting error in data to be transmitted; and

means for applying addresses stored in the address storage device and error detection signals generated by the error detection generation means to the modulation input of the VCO at an amplitude less than the amplitude of the chip code applied to the modulation of the input by the chip code generator, thereby sequentially modulating the output frequency of the voltage controlled oscillator less broadly than when the chip code alone is applied to the modulation input of the voltage controlled oscillator.

45. The spread spectrum transmitter according to claims 34, 35 or 36, further comprising:

multiplication means for multiplying the frequency output by the voltage controlled oscillator by a predetermined integer multiple of the frequency of the voltage controlled oscillator to produce a desired carrier frequency.

46. The spread spectrum transmitter according to claim 38, further comprising:

means for limiting a length of a data message transmitted so that once initial spread spectrum synchronization is achieved by a receiver, a receiver can run open loop without performing chip code synchronization.

47. The transmitter of Claims 34, 35 or 36, further comprising:

said chip code generator means generating a chip code sequence repetition at a chip rate of approximately 1.0-1.3 Mc/s

to produce a frequency shift keying (FSK) spread spectrum modulated signal.

48. A spread spectrum transmitter comprising:

carrier generation means for generating a modulated carrier signal, said carrier generation means including a modulation input for application thereto of a modulating signal;

a buffer amplifier, having an enable input, for amplifying the modulated carrier signal generated by said carrier generation means;

a filter connected to an output of the buffer amplifier for filtering the output of the buffer amplifier;

an antenna connected to an output of the filter;

processor means for controlling transmissions by said carrier generation mean, including,

processor oscillator means for producing a reference signal for stabilizing the carrier signal,

means for stabilizing the carrier signal by means of the reference signal produced by said processor oscillator means, and

chip code generator means clocked by the processor oscillator means for producing a chip code signal applied to the modulation input of said carrier generation means, thereby producing at the antenna a spread spectrum carrier frequency coherently locked to chip code generation means;

timer means for defining a low current inactive mode and an active operating mode in which the processor means, the carrier generation means and the amplifier are enabled;

wake-up means having an external input and a timer input from said timer means for enabling said processor means, carrier

generation means and amplifier means in accordance with the external input and the input from the timer means; and

said processor means further comprising means for generating plural active mode transmit messages thereby providing transmitted message redundancy.

49. The transmitter of Claim 48, wherein said processor means comprises:

means for applying a data message to the modulation input of said carrier generation means; and

means for limiting the length of the data message so that once initial spread spectrum synchronization is achieved by a receiver, the receiver can run open loop without performing continuous chip code synchronization.

50. The transmitter of Claims 48 or 49, wherein said carrier generation means comprises:

a voltage controlled oscillator having a modulation input modulated by said processor means to produce a FSK modulated signal.

51. The transmitter of Claim 48, wherein said carrier generation means comprises:

a tuned oscillator; and

a phase shift keyed modulator coupled to said tuned oscillator and having a modulation input modulated by said processor means to produce PSK modulated signal.

52. The transmitter of Claim 49, wherein said carrier generation means comprises:

a tuned oscillator; and

a phase shift keyed modulator coupled to said tuned oscillator and having a modulation input modulated by said processor means to produce PSK modulated signal.

53. The transmitter of Claims 48 or 49, further comprising:

said chip code generator means generating a chip code sequence at a chip rate of approximately 1.0-1.3 Mc/s to produce a frequency shift keying (FSK) spread spectrum modulated signal.

54. The transmitter of Claims 28, 51 or 52, further comprising:

said chip code generator means generating a chip code sequence at a chip rate of approximately 1.0-1.3 Mc/s to produce a phase shift keying (PSK) spread spectrum modulated signal.

55. A spread spectrum transmitter comprising:

oscillator means, including a voltage controlled oscillator having a modulation input, for generating a transmitter output at a carrier frequency;

processor means for controlling transmissions by the voltage controlled oscillator, said processor means including processor oscillator means for producing a frequency stabilizing reference clock signal;

means for stabilizing the frequency of the voltage controlled oscillator by locking the frequency of the voltage controlled oscillator to the frequency stabilizing reference clock signal produced by said processor oscillator means; and

said processor means further comprising chip code generator means clocked by the processor oscillator means for generating a chip code signal applied to the oscillator means, thereby locking the transmitter carrier frequency to the processor

reference clock signal with the processor reference clock in a fixed relationship with the carrier frequency.

56. The transmitter of Claim 55, further comprising:

said chip code generator means generating a chip code sequence repetition at a chip rate of approximately 1.0-1.3 Mc/s to produce a frequency shift keying (FSK) spread spectrum modulated signal.

57. The transmitter of Claim 55, wherein said carrier generation means comprises:

a tuned oscillator; and

a phase shift keyed modulator coupled to said tuned oscillator and having a modulation input modulated by said processor means to produce PSK modulated signal.

58. The transmitter of Claim 57, further comprising:

said chip code generator means generating a chip code sequence repetition at a chip rate of approximately 1.0-1.3 Mc/s to produce a phase shift keying (PSK) spread spectrum modulated signal.

59. The method of Claim 3, wherein the oscillator is modulated with fast frequency shift key (FFSK) modulation.

60. The method of Claim 1, wherein at least one of the data applied to the modulation input causes a priority transmission at an increased rate of message transmission.

61. The method of Claims 1 or 60, comprising:

transmitting repetitively a supervisory message.

62. The transmitter of Claims 12, 21, 29 or 32, wherein at least one of the data applied to the modulation input causes a priority transmission at an increased rate of transmission.

63. The transmitter of Claims 12, 21, 29 or 32, comprising:

means for initiating repetitive transmission of a supervisory message.

64. The transmitter of Claim 62, comprising:

means for initiating repetitive transmission of a supervisory message.

ABSTRACT

A wireless alarm system using spread spectrum transmitters, fast frequency shift keying, spread spectrum receivers and computer with a display. The spread spectrum transmitter includes an oscillator coupled to a microprocessor with chip code generation means, preamble register, address register and data register. The spread spectrum receiver acquires synchronization of the spread spectrum signal using a microprocessor coupled to the quieting, signal strength or baseband output of the receiver, with a two step algorithm. The steps comprise achieving a coarse lock and a fine lock to the spread spectrum signal.

20 CONT

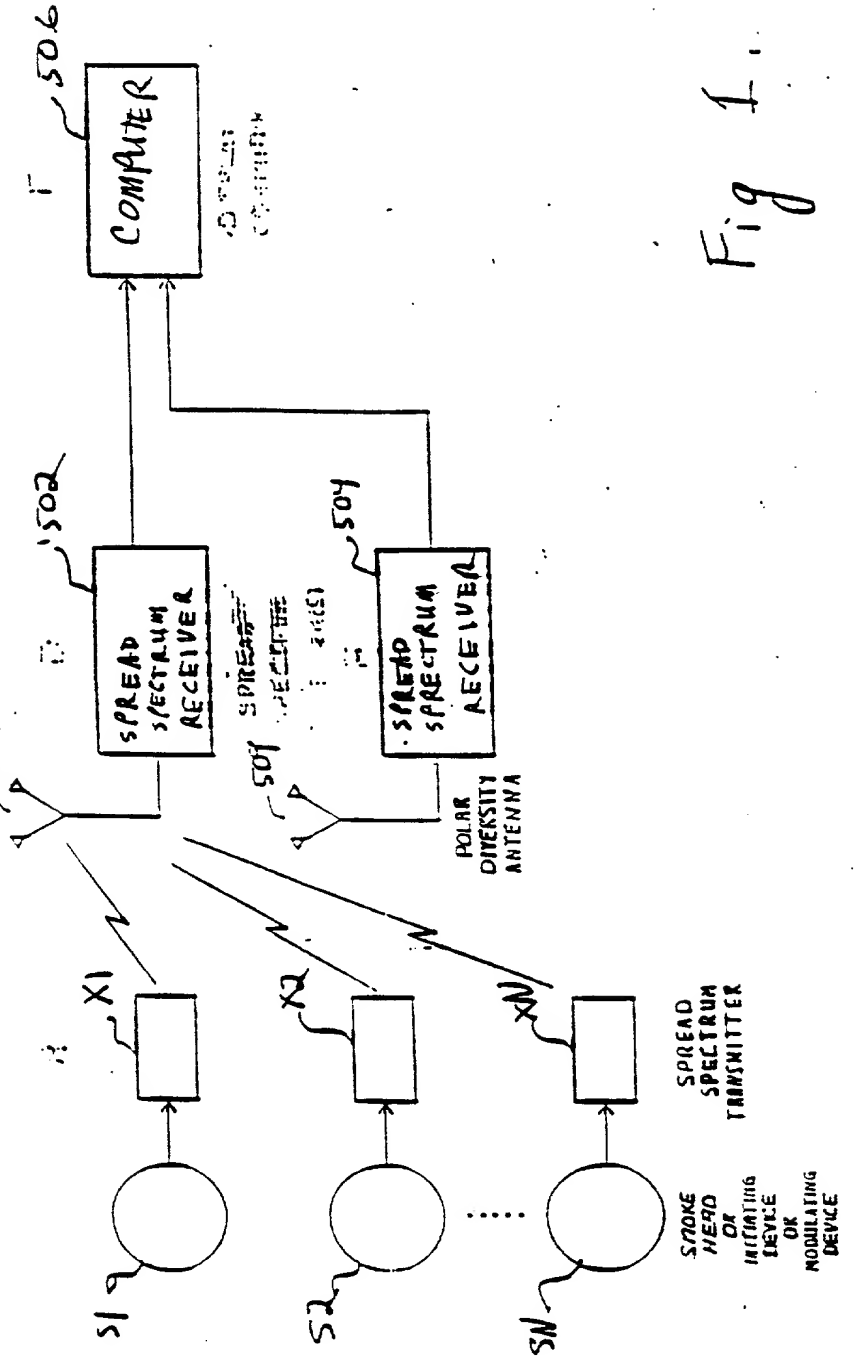
506
COMPUTER
502
SPREAD SPECTRUM RECEIVER
504
SPREAD SPECTRUM RECEIVER
507
507
POLAR DIVERSITY ANTENNA
X1
X2
XN
SPREAD SPECTRUM TRANSMITTER
S1
S2
SN
SMOKE HEAD OR INITIATING DEVICE OR MODULATING DEVICE

Fig 1.

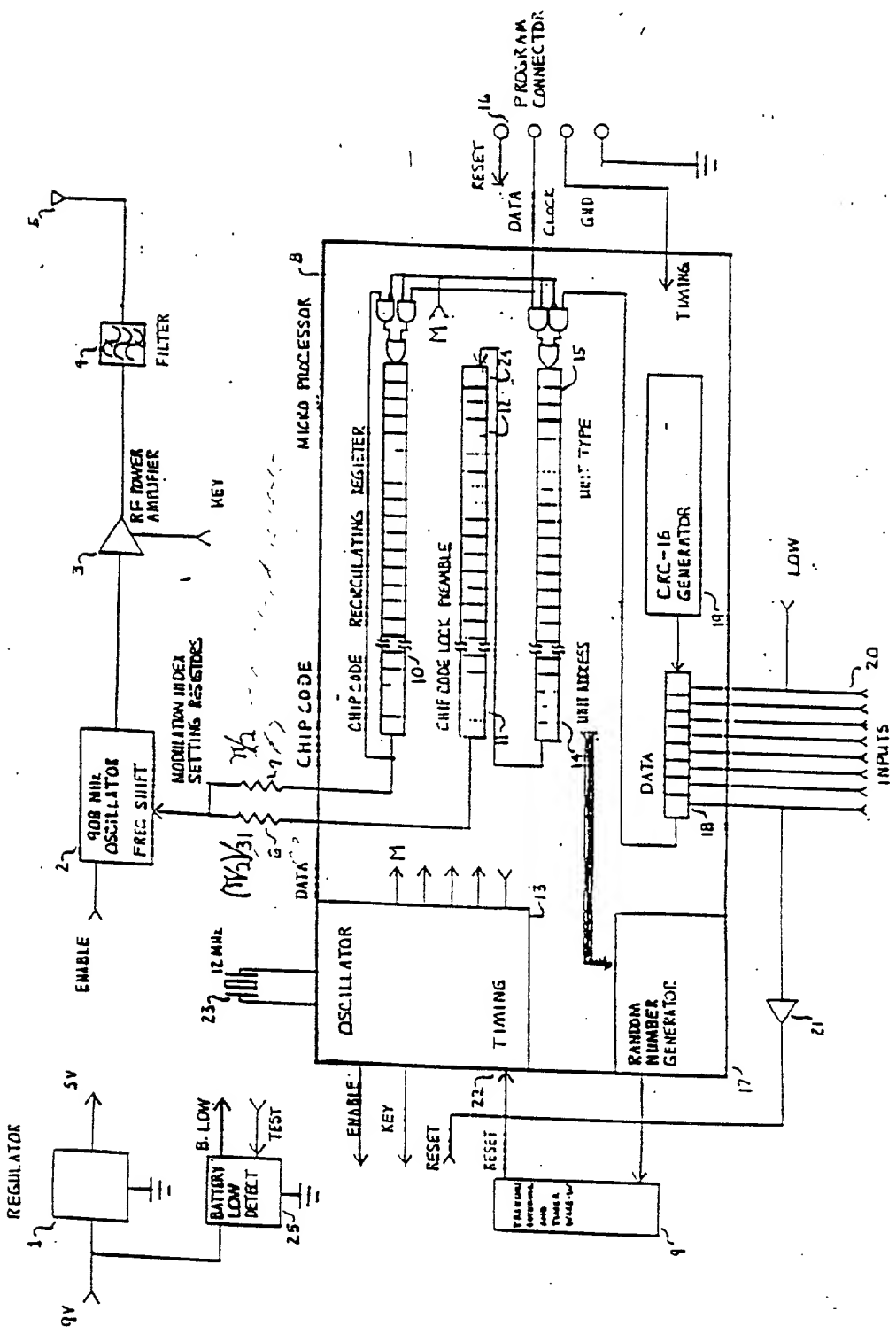
RESET
DATA
CLOCK
GND
PROGRAM CONNECTOR
16
TIMING
MICRO PROCESSOR
8
FILTER
4
5
RF POWER AMPLIFIER
3
KEY
CHIP CODE RECIRCULATING REGISTER
CHIP CODE LOCK PREMBLE
UNIT TYPE
15
CRC-16 GENERATOR
19
LOW
MODULATION INDEX SETTING RESISTORS
CHIP CODE
10
11
14
UNIT ADDRESS
DATA
18
20
INPUTS
908 MHz OSCILLATOR FREQ SHIFT
2
ENABLE
DATA
6
M
13
12 MHz
23
OSCILLATOR
TIMING
RANDOM NUMBER GENERATOR
17
21
REGULATOR
5V
9V
1
B. LOW
TEST
BATTERY LOW DETECT
25
ENABLE
KEY
RESET
22
RESET
9

Fig. 2

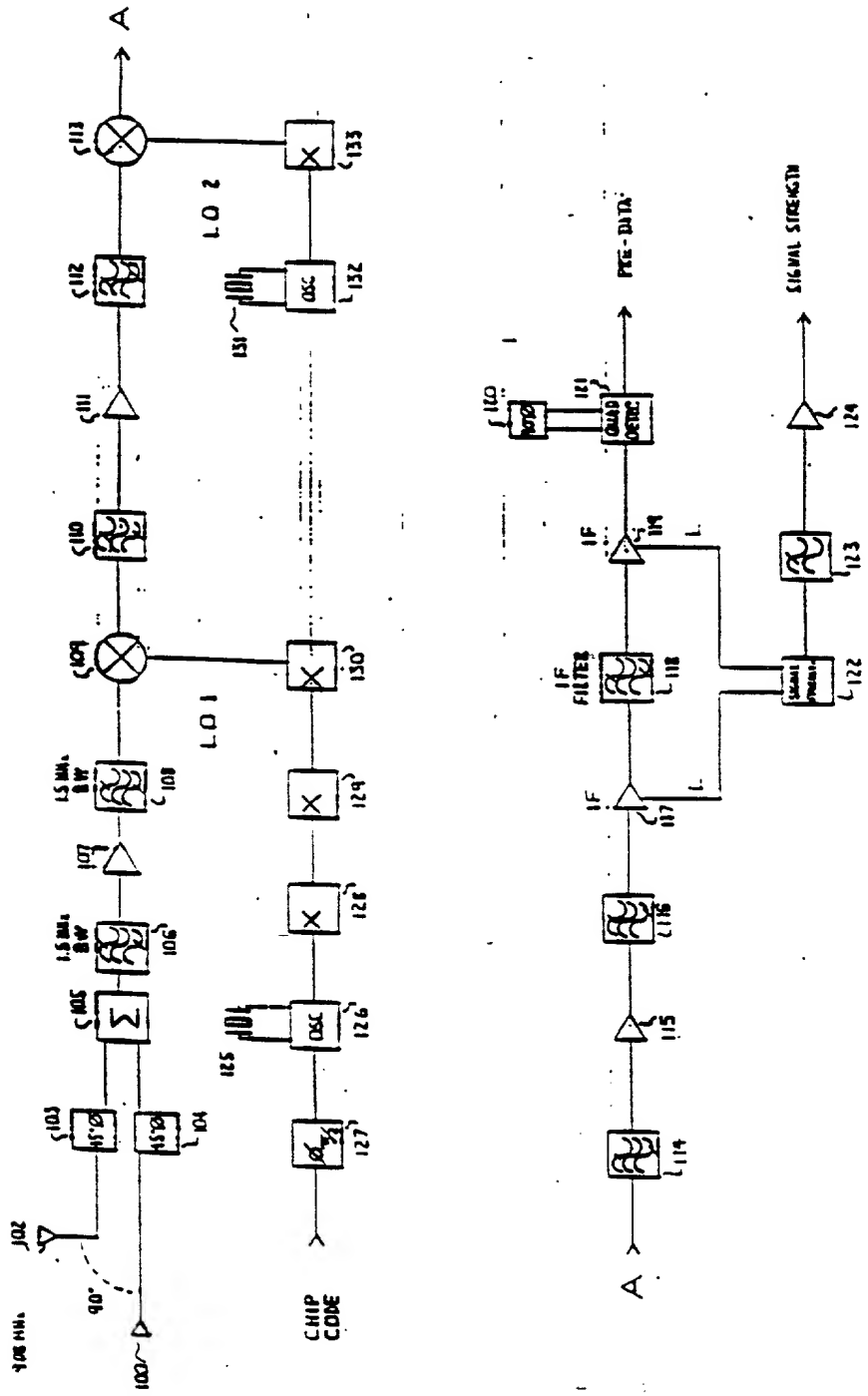

Fig. 3A

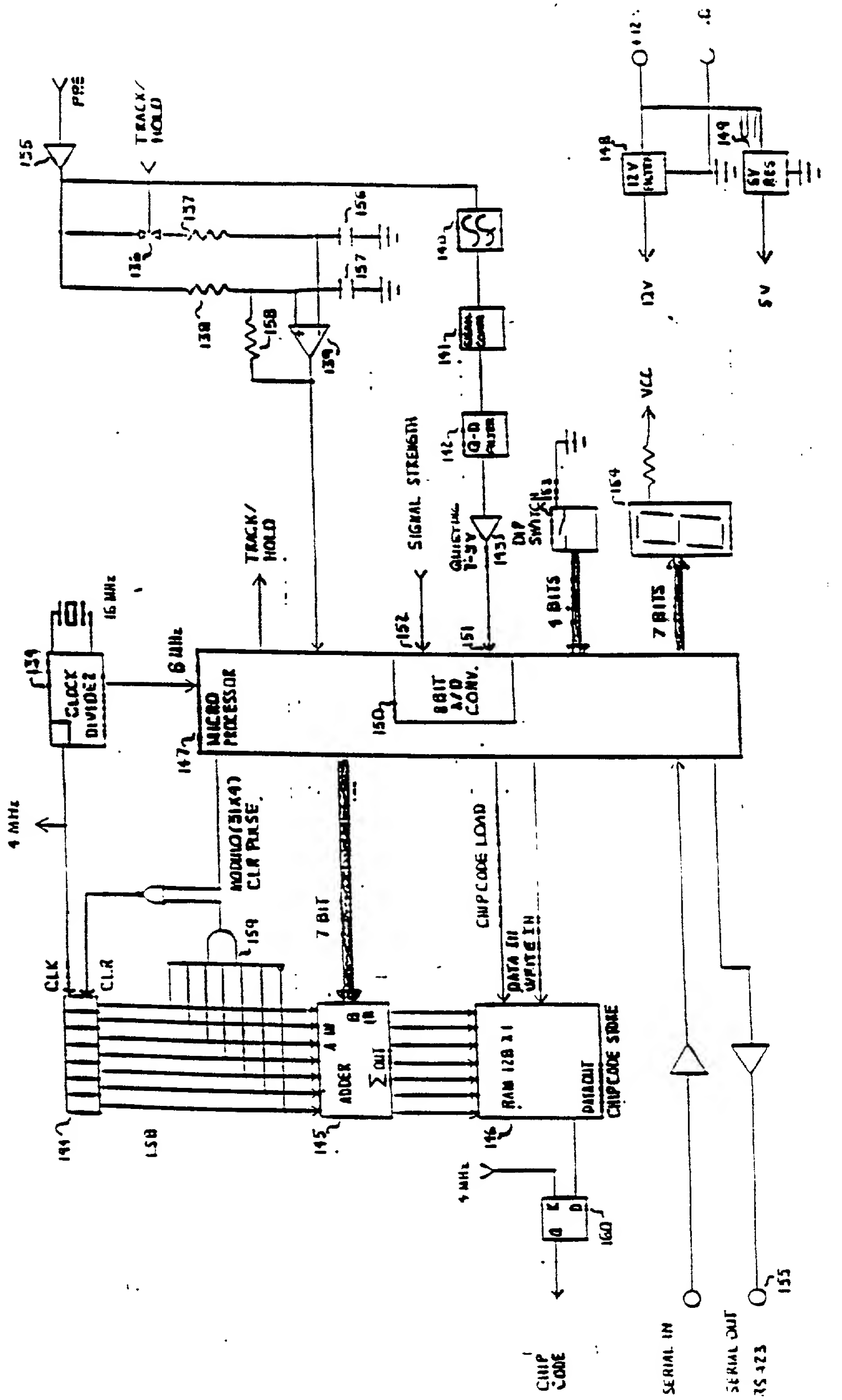
TRACK/HOLD
CLOCK DIVIDER
16 MHz
6 MHz
4 MHz
MICRO PROCESSOR
8 BIT A/D CONV.
TRACK/HOLD
SIGNAL STRENGTH
QUIETING 1-5V
DIP SWITCH
4 BITS
7 BITS
VCC
12V
5V
MODULO(31X4) CLR PULSE
CLK
CLR
LSB
7 BIT
ADDER
CHIPCODE LOAD
DATA IN
WRITE EN
RAM 128 X1
DATA OUT
CHIPCODE STORE
4 MHz
CHIP CODE
SERIAL IN
SERIAL OUT RS 423

Fig 3B

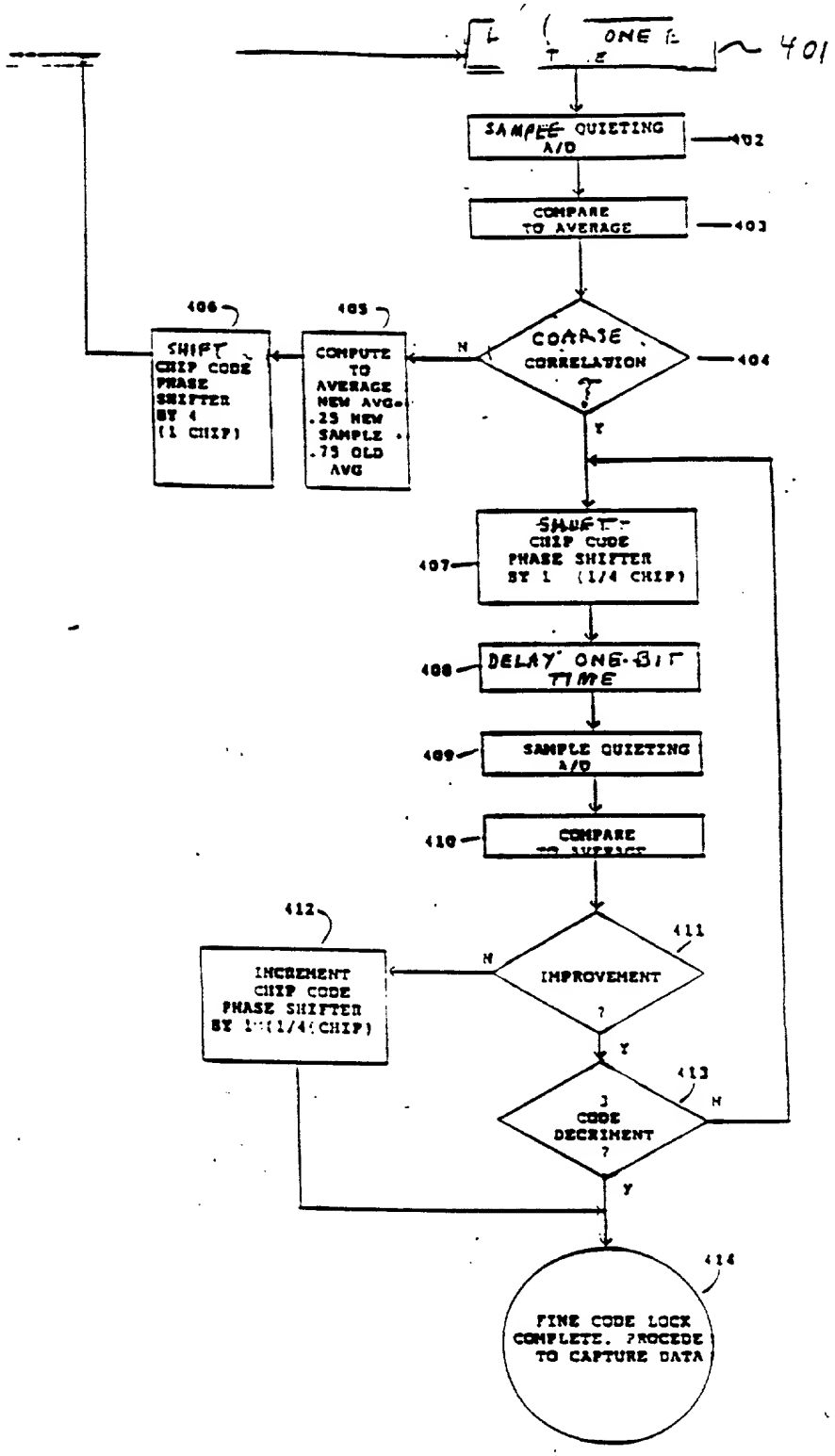
401
SAMPLE QUIETING A/D
402
COMPARE TO AVERAGE
403
COARSE CORRELATION
404
N
Y
405
COMPUTE NEW AVERAGE NEW AVG= .25 NEW SAMPLE + .75 OLD AVG
406
SHIFT CHIP CODE PHASE SHIFTER BY 4 (1 CHIP)
SHIFT CHIP CODE PHASE SHIFTER BY 1 (1/4 CHIP)
407
DELAY ONE-BIT TIME
408
SAMPLE QUIETING A/D
409
COMPARE
410
IMPROVEMENT
411
INCREMENT CHIP CODE PHASE SHIFTER BY 1 (1/4 CHIP)
412
CODE DECREMENT
413
FINE CODE LOCK COMPLETE. PROCEDE TO CAPTURE DATA
414

Fig. 4

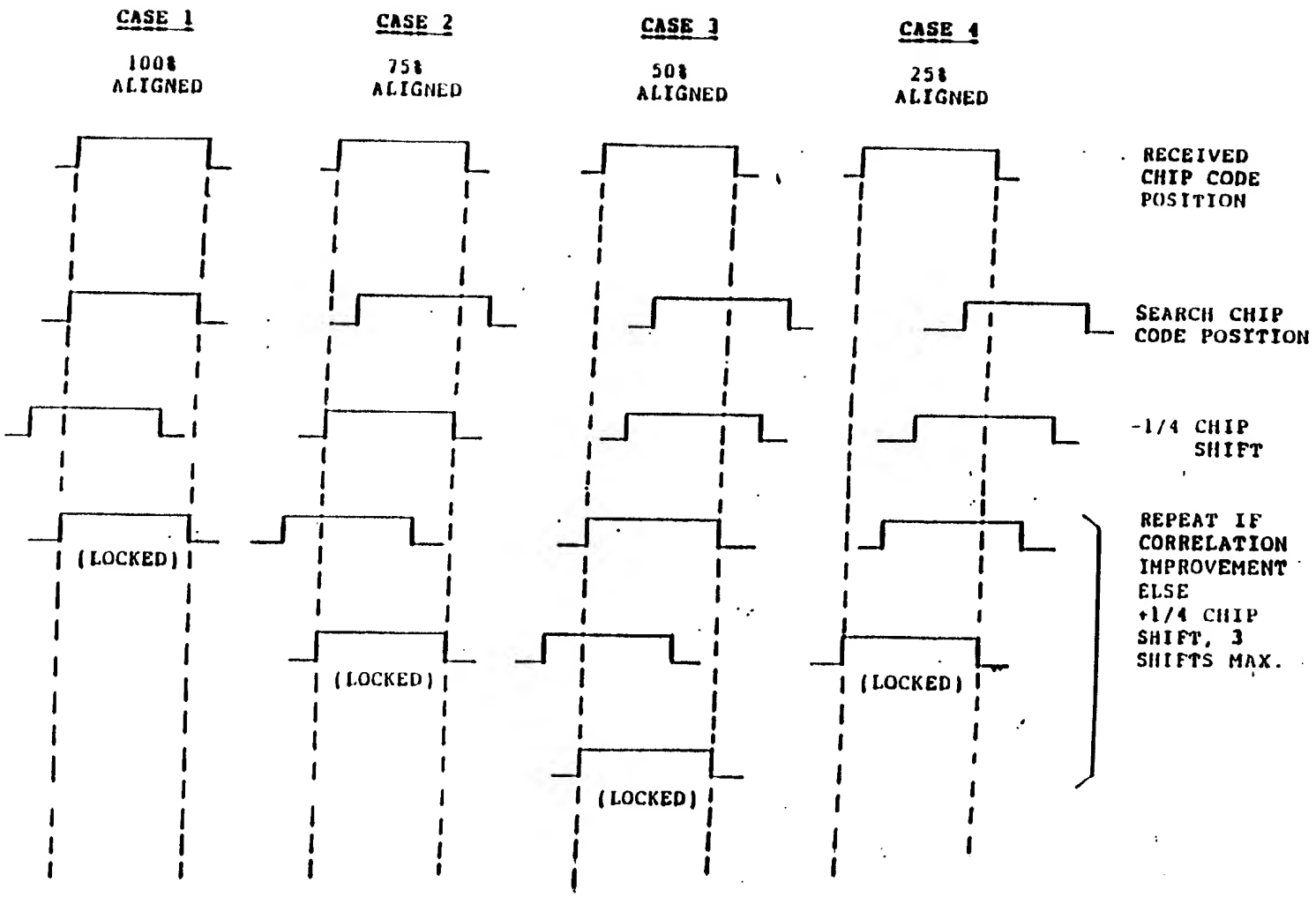

Fig 5

20 CONT

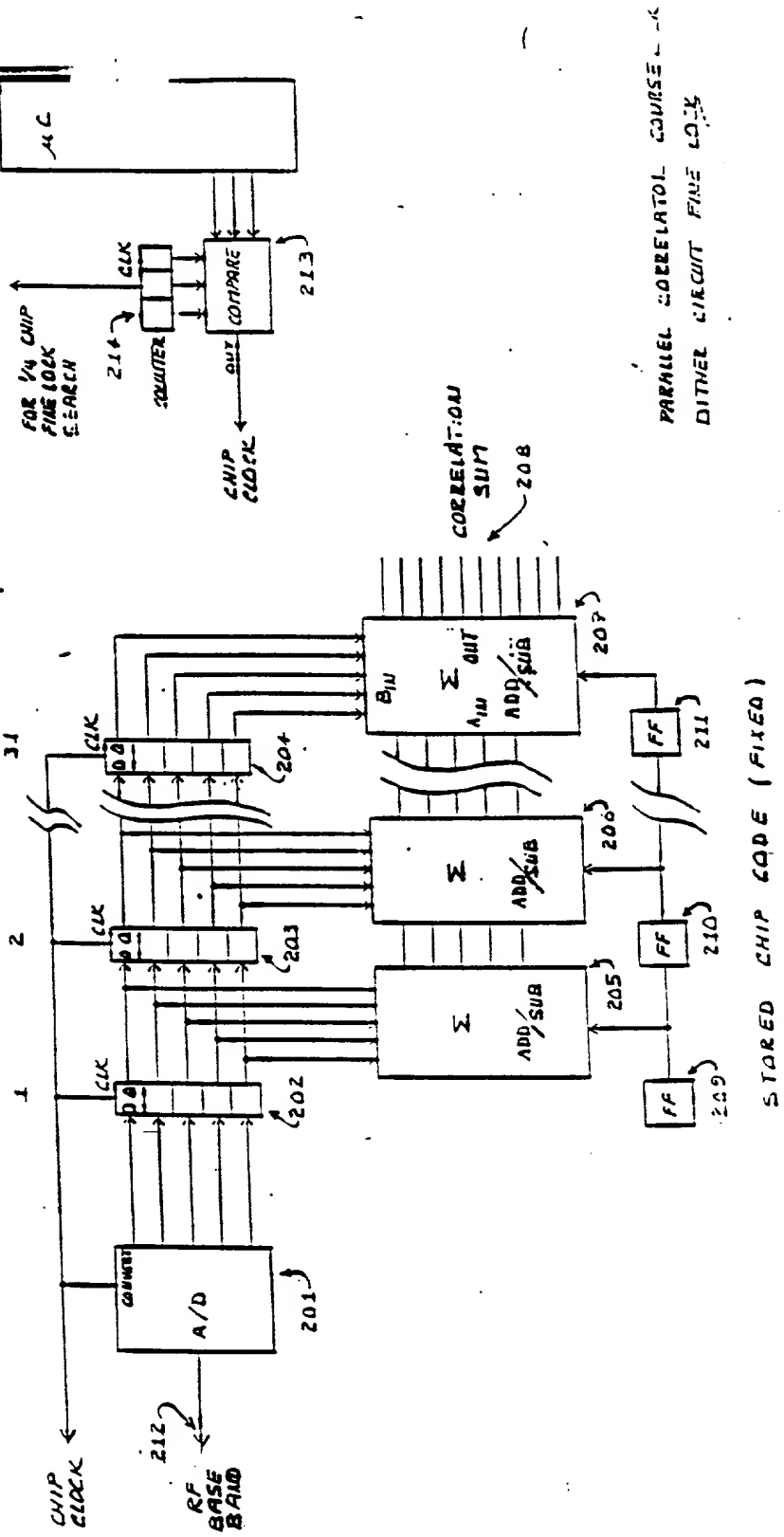
μC
215
4X CHIP RATE
FOR 1/4 CHIP FINE LOCK SEARCH
CLK
COUNTER
214
COMPARE
OUT
213
CHIP CLOCK
CORRELATOR SUM
208
PARALLEL CORRELATOR COARSE
DITHER CIRCUIT FINE LOCK
STORED CHIP CODE (FIXED)
A/D
201
202
203
204
205
206
207
210
211
209
ADD/SUB
Σ
OUT
CHIP CLOCK
RF BASE BAND
212

Fig 6

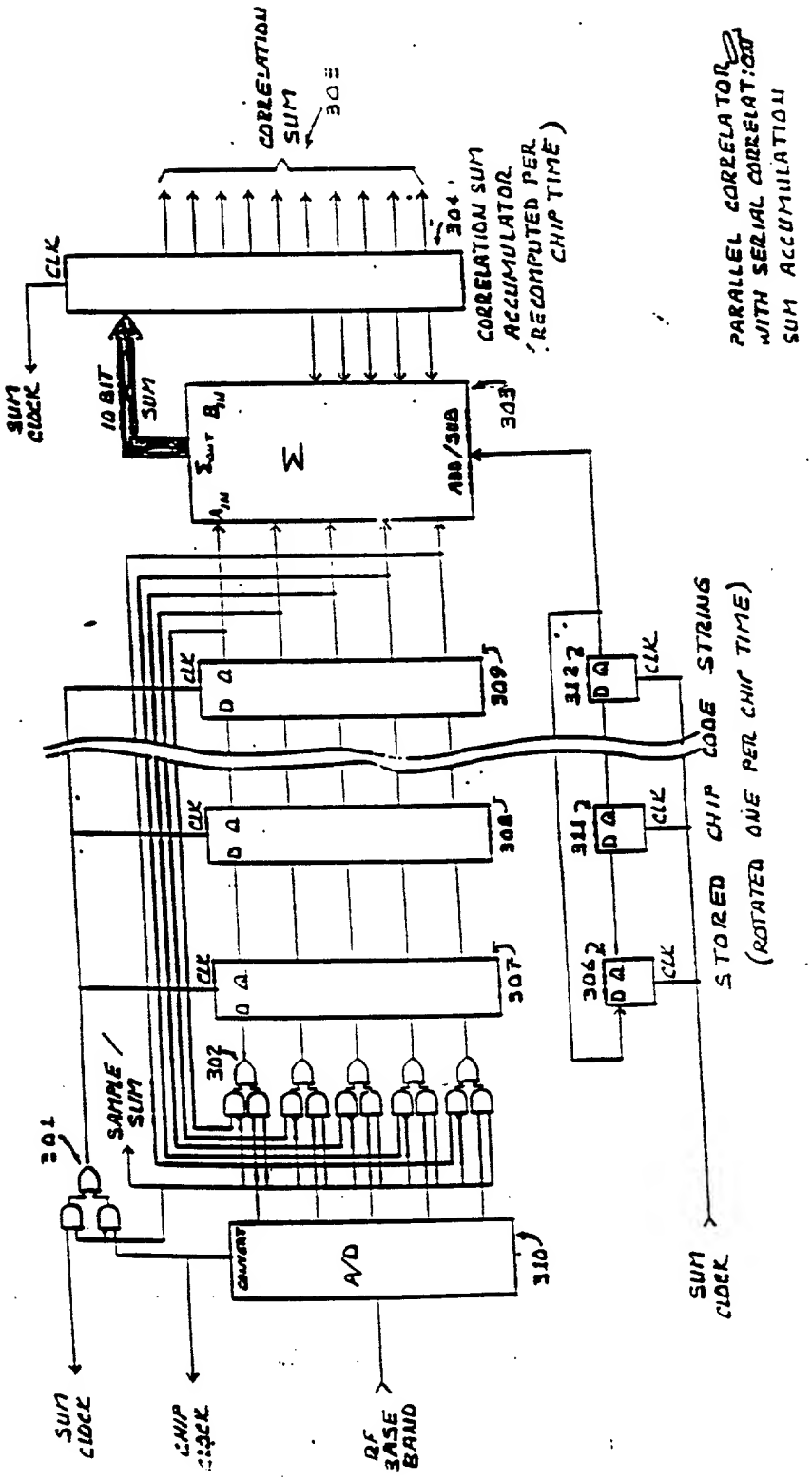
CORRELATION SUM
302
304
CLK
SUM CLOCK
10 BIT SUM
CORRELATION SUM ACCUMULATOR (RECOMPUTED PER CHIP TIME)
303
ADD/SUB
309
308
307
312
311
306
CODE STRING
STORED CHIP (ROTATED ONE PER CHIP TIME)
SAMPLE / SUM
301
A/D
310
SUM CLOCK
CHIP CLOCK
RF BASE BAND
PARALLEL CORRELATOR WITH SERIAL CORRELATION SUM ACCUMULATION

Fig 7.